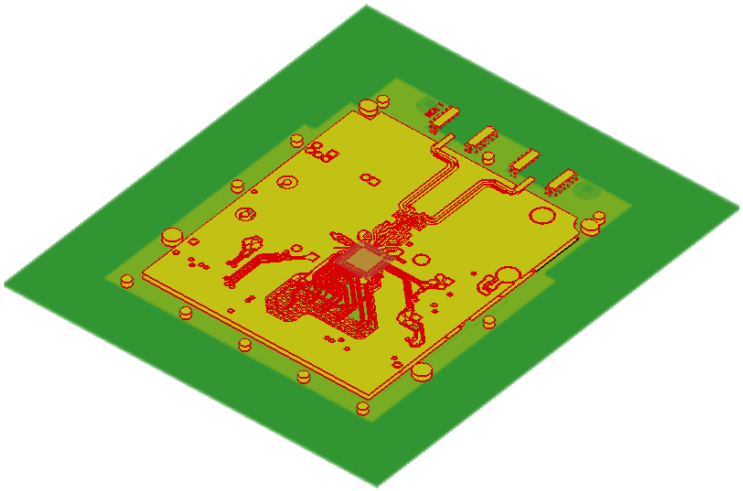
PCB Simulation in Wavenology EM



Wave Computation Technologies, Inc.

Aug. 2018

Outline

- Requirements
  - Version of Wavenology EM
  - PCB models
  - Schematic Circuit of the PCB or the layout of lumped elements in the PCB
  - Miscellaneous
- Basic steps to set up a PCB simulation model
- Demo
  - Simulation on the DC2266A Evaluation Board

Requirements

We assume that the users have already known how to use Wavenology EM to simulate the regular EM applications, including the usage of lumped elements (R, L, C, diode & Spice circuit). If the users do not have the above experience, please refer to the manual of Wavenology EM.

- Version of Wavenology EM
  - It must be a version >= 2.0.6, which is released in August 2018

- PCB models
  - The Gerber file for each layer of the PCB board
    - It should be the version RS-274X. The old versions, for example, RS-274D, is not fully tested (some deprecated keywords are not supported)
  - The Excellon-like drill file, if user need to connect layers by via
    - Wavenology EM does not fully support a Excellon drill file with all Excellon features, it only supports the drilling information. This is the drill file exported from most popular EDA software. It has passed the test for the drill file exported from Cadence Allegro
    - User need to know which two layers that a drill file will connect
  - The thickness and the electric properties of each substrate layer

- Schematic Circuit of the PCB or the layout of lumped elements in the PCB
  - In general, there are lumped elements in the PCB, but the Gerber file may not include that information. In order to build a fully functional PCB, user need to have the circuit scheme for the board, or the layout image of the board, to include the information of all lumped elements.

- Miscellaneous
  - IBIS data file for the chips in the board
  - The physical size of the chip & the layout of pins for the chip in the board
    - If there are chips in the board, sometimes, the Gerber model can't provide enough information for the pad for pins. Wavenology EM GUI allow user to load the IBIS information for the chip and define an image for the layout of pins, which can make the connection of traces more clear.

Basic Steps to Set up a PCB Simulation Model

1. Prepare the PCB model for each layer – Gerber files, RS-274X format
2. Prepare the drilling model for via – Excellon-like drill files
3. Obtain the layer position & the material parameters for substrates
4. Prepare the Schematic Circuit of the PCB or the layout of lumped elements in the PCB – which is used to know the parameters of the lumped elements and the layout in the board
5. Insert the PCB model in (1) into the Wavenology EM project
6. Insert the Drilling model in (2) into the Wavenology EM project

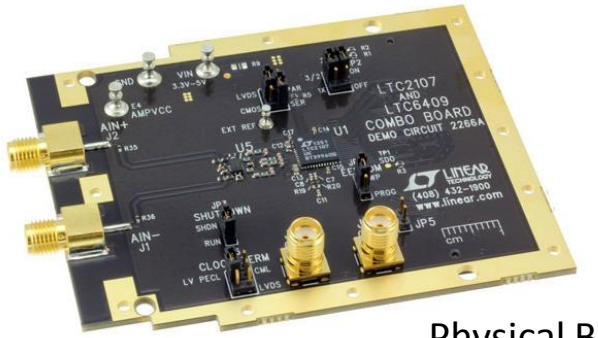
7. Shift PCB layers & Drilling layers to the correct Z positions
8. “Thicken” the drilling model to convert the drilling hole to PEC via
9. Build substrate layers
10. Place lumped elements in the PCB model
11. Define excitation(s)
12. Define monitoring parameters

Demo

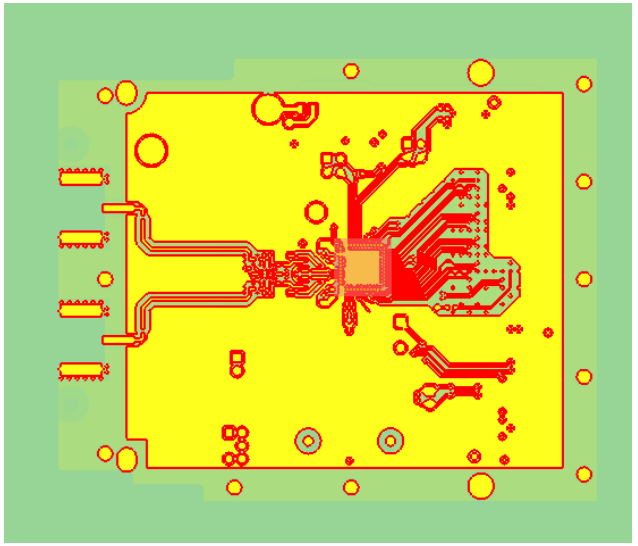
Simulating the DC2266A Evaluation Board

- In this demo, we will show the steps to set up a 3D EM simulation from the PCB models
  - 6 layers PCB
  - a full functional ADC application for chip LTC2107

- We will show how to simulate the signal propagation from the input connector of the board



Physical Board



Simulation Model

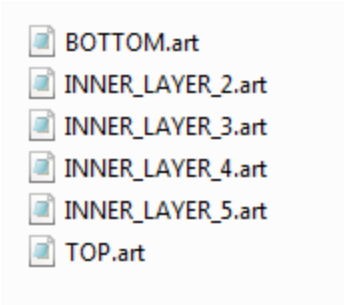
1. Obtain the PCB model & the chip model from **analog.com**

- The documentation for PCB are available from
  - http://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/dc2266a.html#eb-overview
    - ❑ the Design Files include a PCB project from EDA software, and Gerber files for each layer, Drill files and other information
      - ○ however, it seems that the Drill files in the package has a different coordinates system with the Gerber files, and the Drill file does not include enough drill-bit-switching information. So, we recommend to use the PCB project to re-export the Gerber file and the Drill file with newest Cadence Allegro to make the models better.
    - ❑ Schematic circuit
    - ❑ Manual: it provides the parameters of all lumped elements in the board

- The documentation for LTC2107 are available from
  - http://www.analog.com/en/products/ltc2107.html#product-overview
    - ❑ user can download the IBIS data file and the data sheet. The data sheet has the physical size and the pin layout of the chip

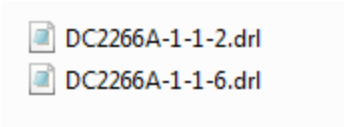
2. Before building a 3D model for the PCB in Wavenology EM, we need to make sure that, at least, following data are available

a) Gerber files for each PCB layer: totally 6 files, as following



the file name shows the layer information

b) Drill files to connect layers



the file name has the information for layer connection

c) The thickness and the dielectric constant of substrate

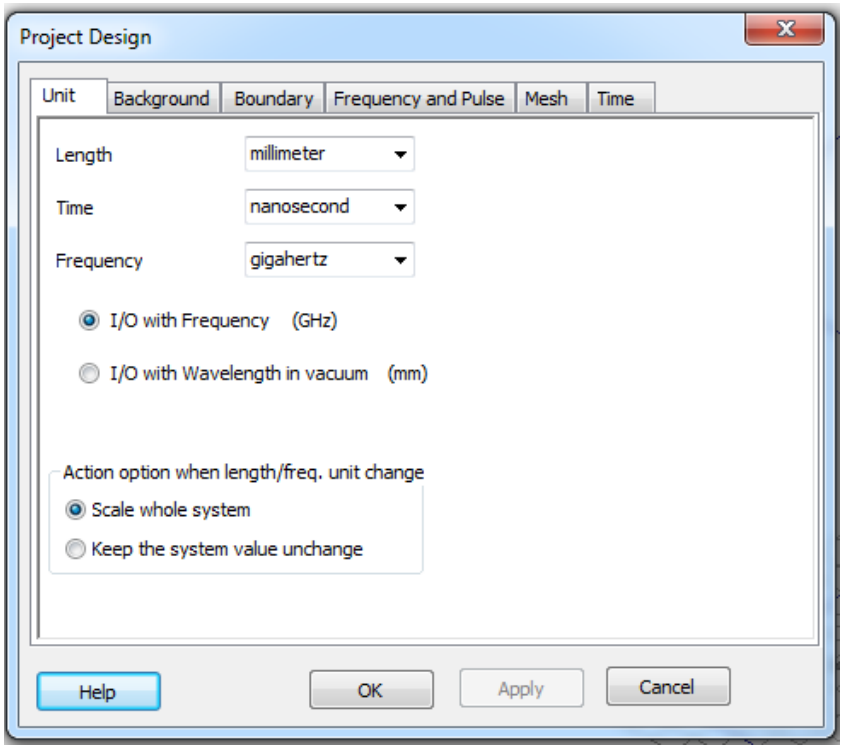
Layer #	Color	Layer Icon	Layer Name	Thickness(...	Material	Conductivity(S...	Fill-in Dielectric	Er	Loss Tangent
1			Signal$Top	0.03429		5.8e+007		[1]	[0]
			Medium$Dielectric1	0.254		0		4.3	0
2			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric3	0.254		0		4.3	0
3			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric5	0.254		0		4.3	0
4			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric7	0.254		0		4.3	0
5			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric9	0.254		0		4.3	0
6			Signal$Bottom	0.03429		5.8e+007		[1]	[0]

d) The parameters of each lumped element and the layout in board

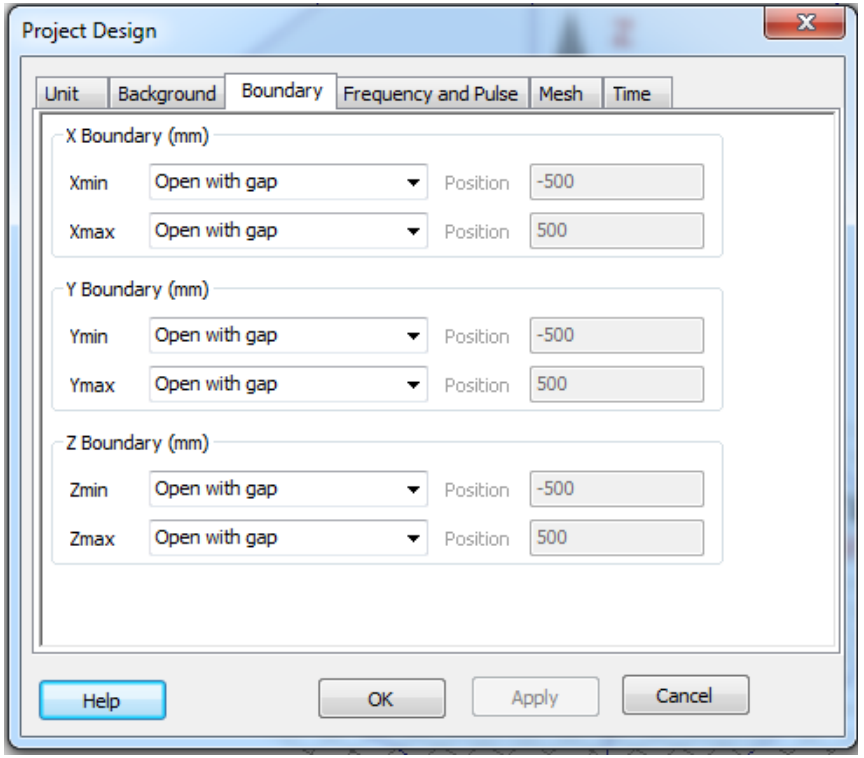
➢ The IBIS data and chip information are optional, not essential, data

3. Setup a **default** EM project in GUI, save as "*dc2266.wnt*".

Project unit use default settings

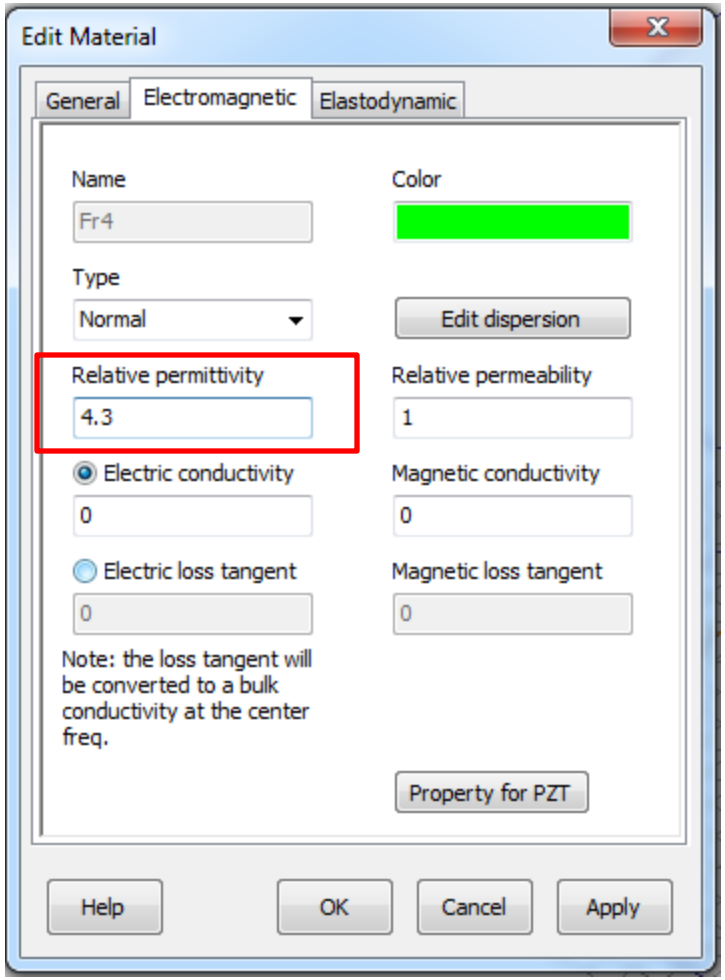


Boundary conditions use default settings:
"Open with gap"

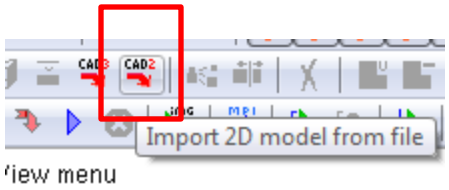


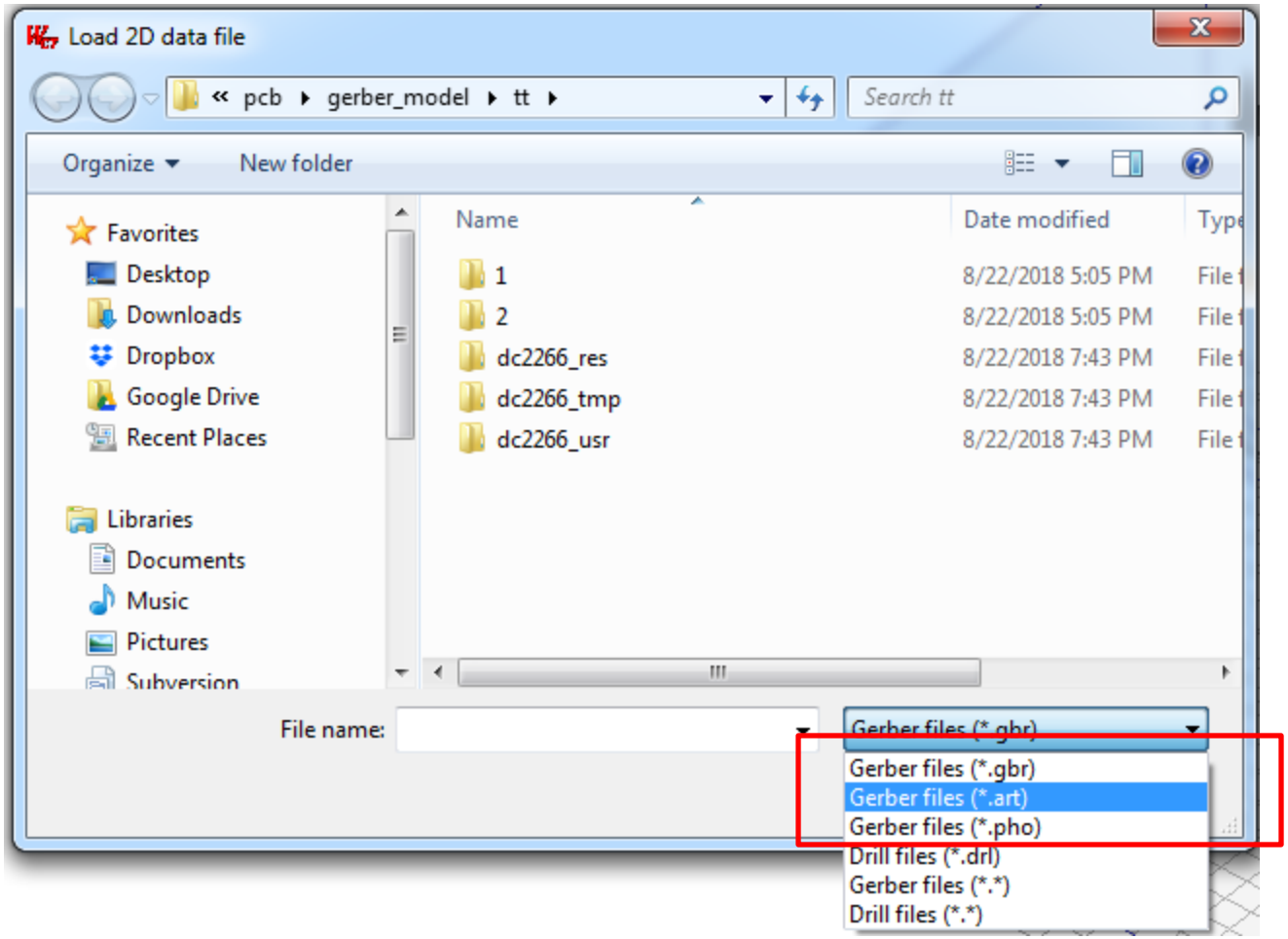
Background material is "Air"

4. Create a new material “Fr4” for substrate, ε_r=4.3



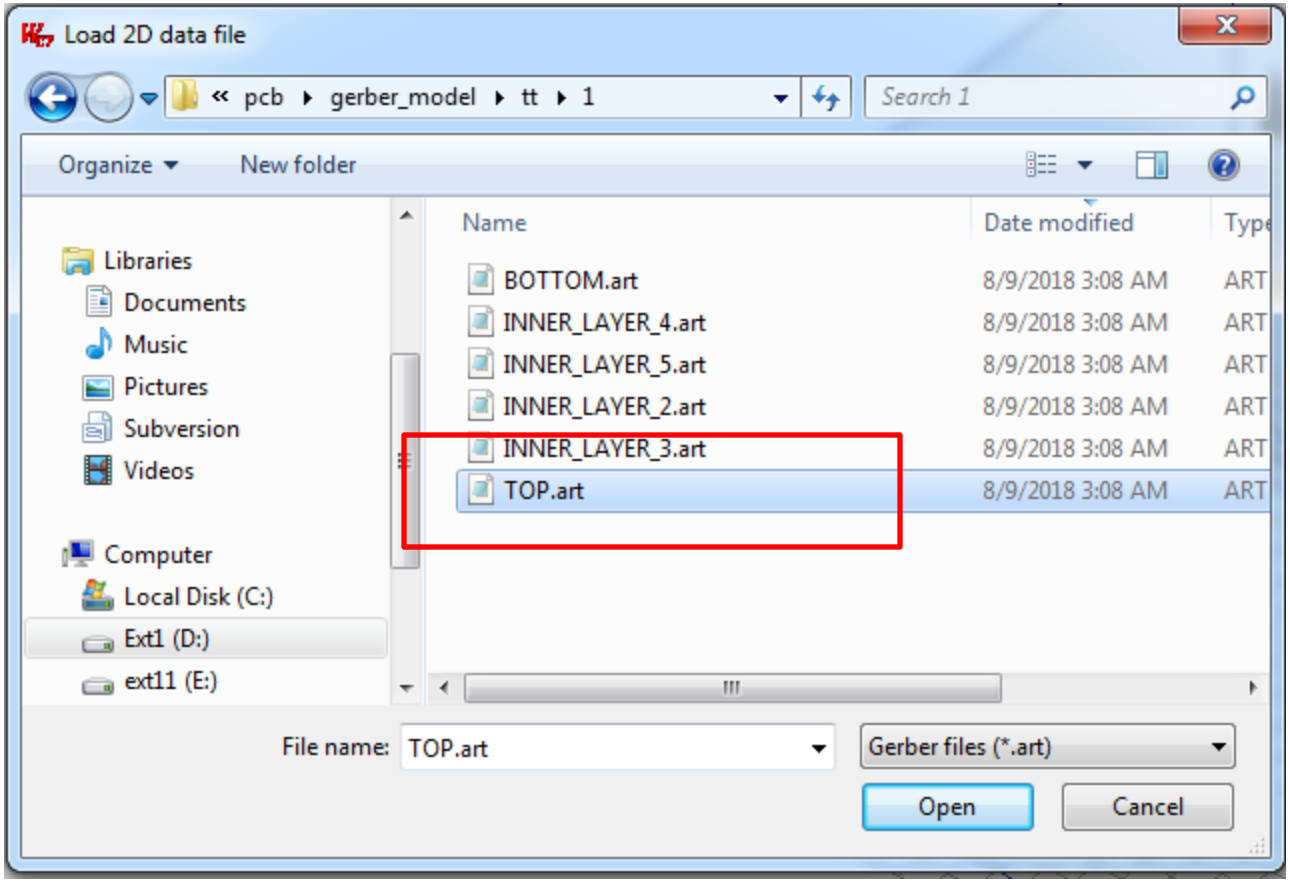
5. Import PCB layers



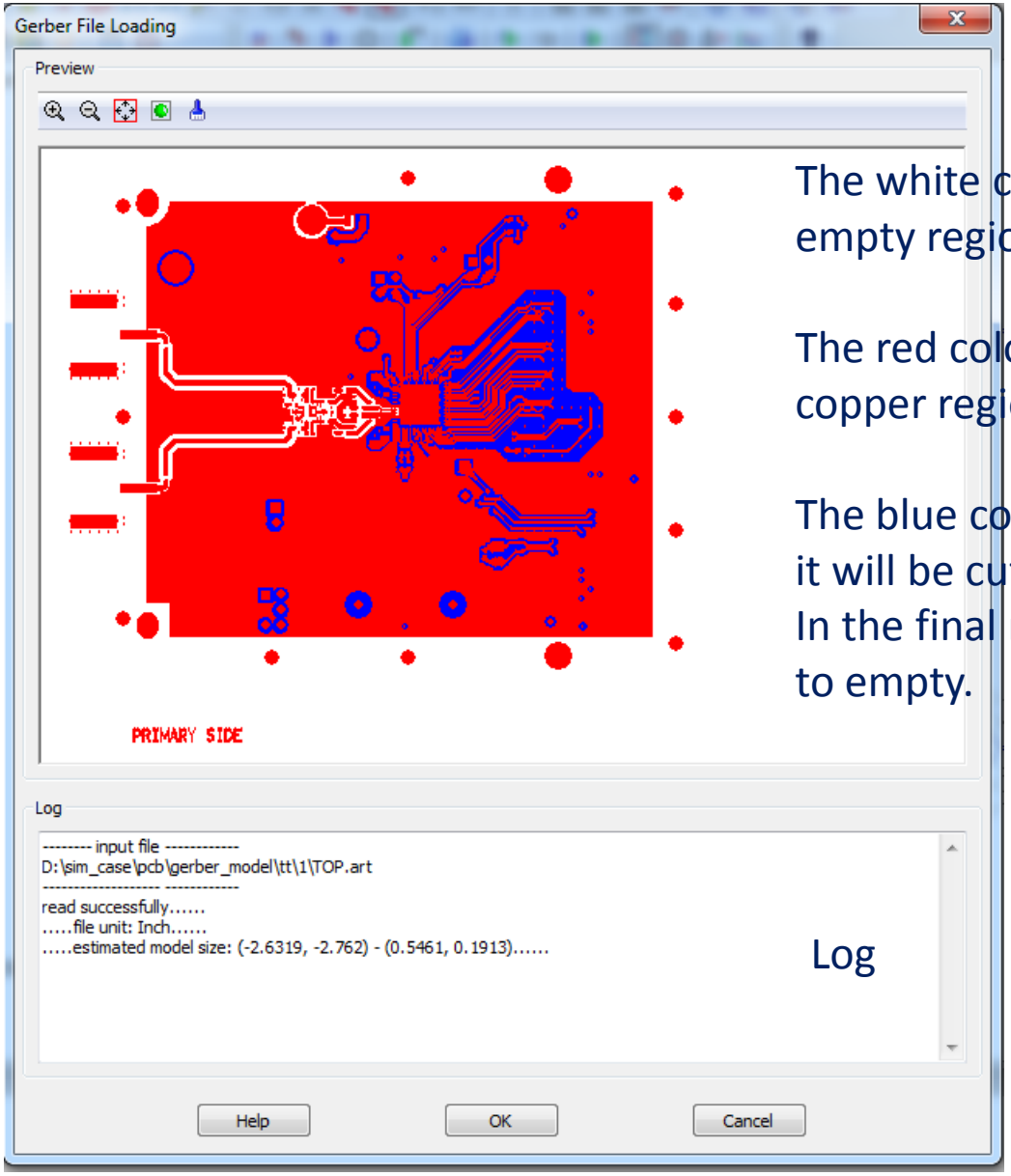


the Gerber files for this case have a suffix as "**art**"

load the ***top*** layer



A preview dialog will be popped up, user can check the model in canvas.



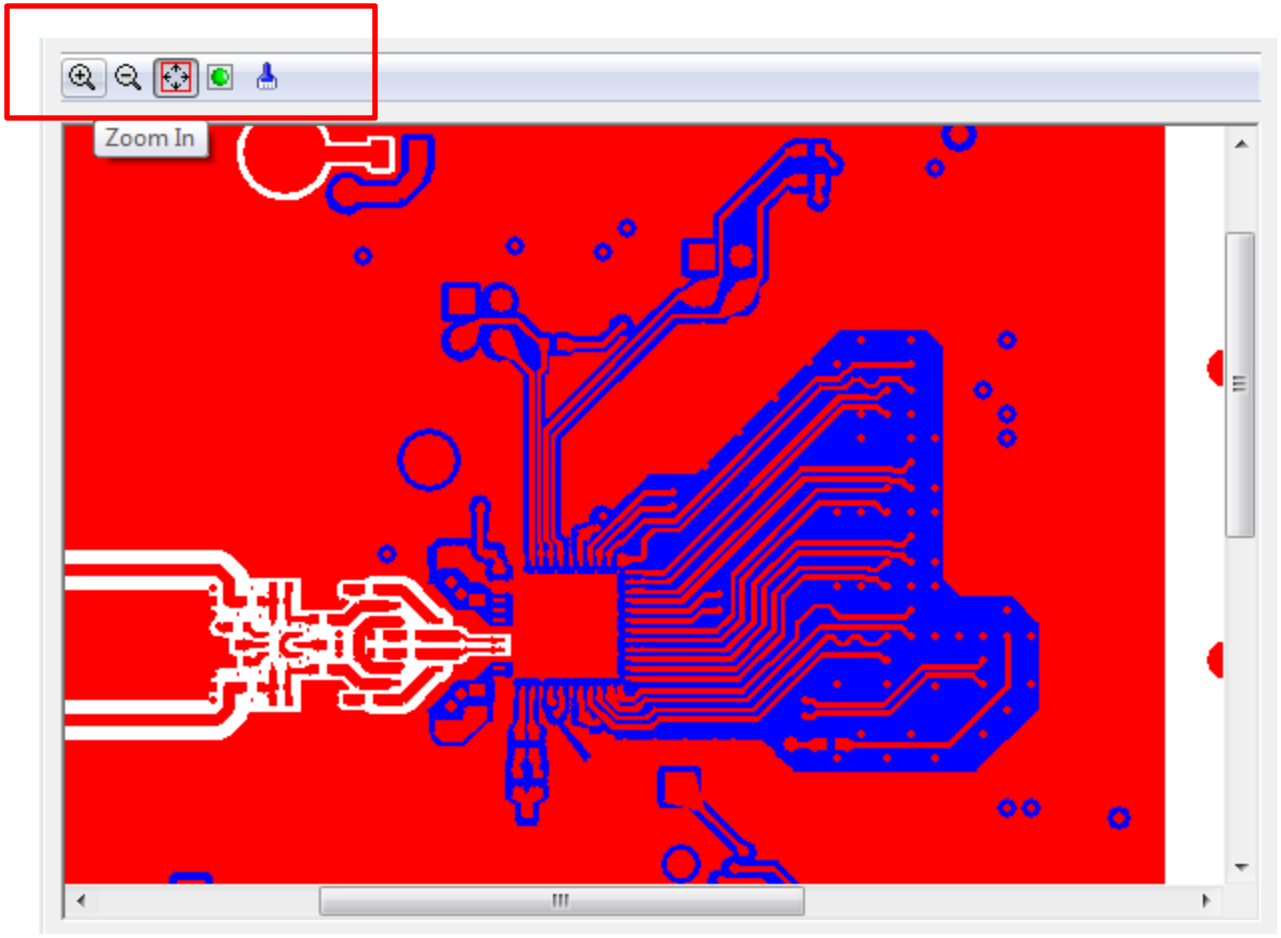
The white color means the empty region.

The red color means the copper region.

The blue color means that it will be cut from model. In the final model, it equals to empty.

Log

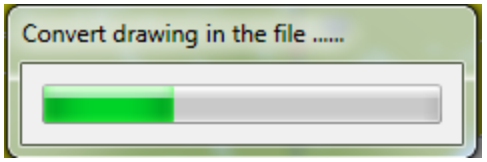
User can check the figure in canvas

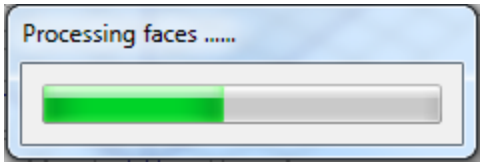


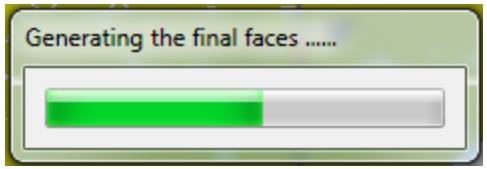
If everything is fine, press the “OK” button to insert the model into the project

Note:

1. This procedure may take a few seconds. The time will depend on the complexity of the model. 3 Progress bars will be shown sequentially to report the progress.



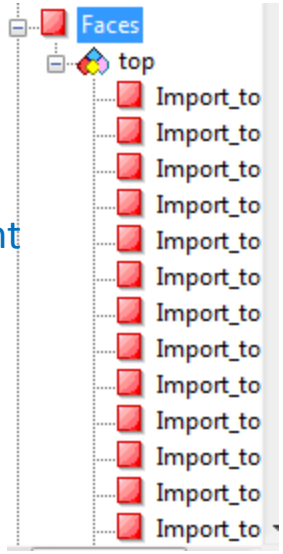


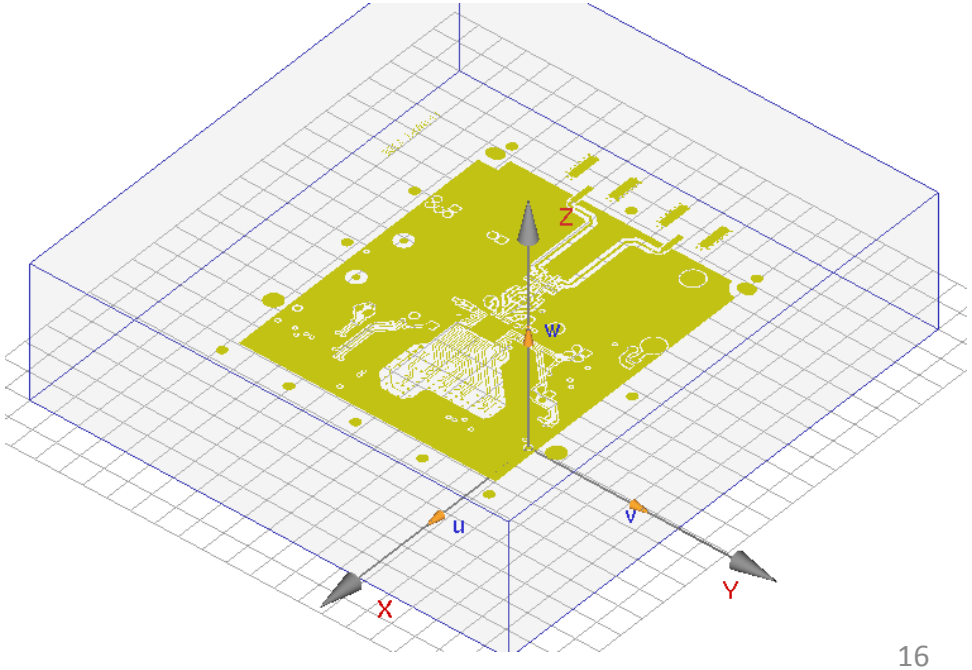


2. The Gerber file does not include Z position of the model. So, after loading, the imported model will be defined as 2D planar faces with Z=0. For convenience, Wavenology set the imported 2D face with the material “PEC”.

After “top” layer loaded

All faces are under the face component “top”





We can repeat this procedure to load other layers:

INNER_LAYER_2

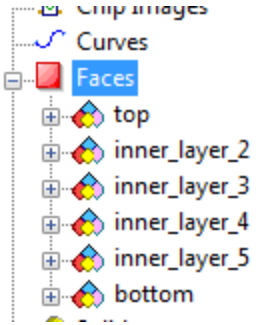
INNER_LAYER_3

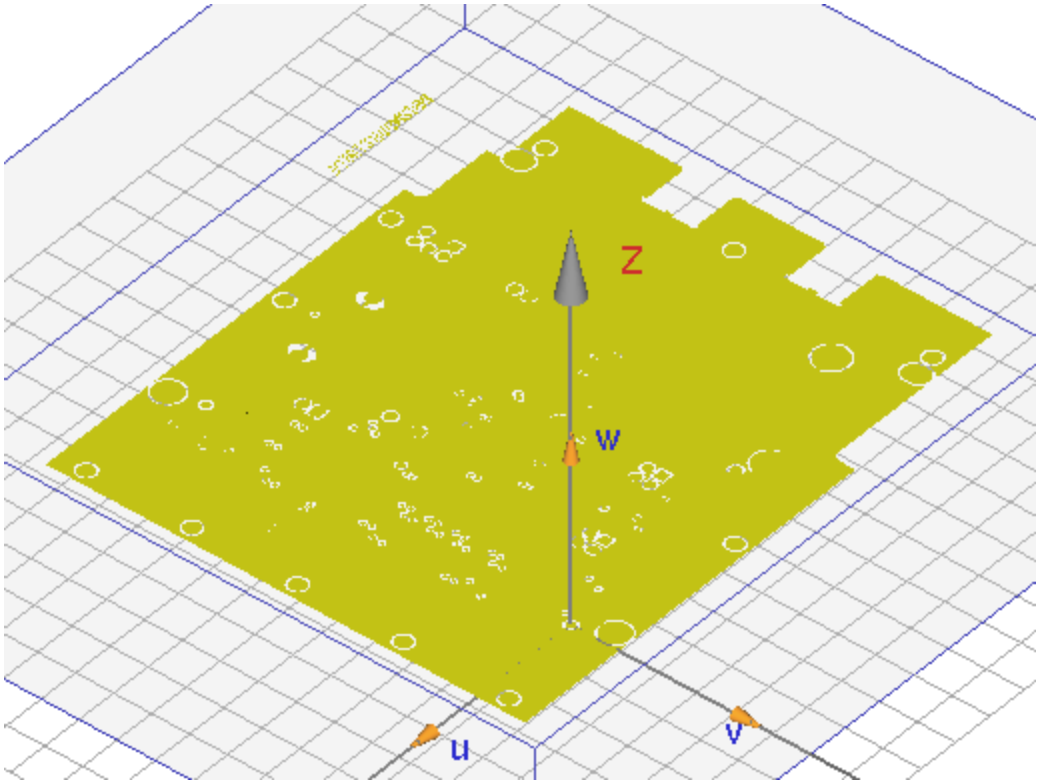
INNER_LAYER_4

INNER_LAYER_5

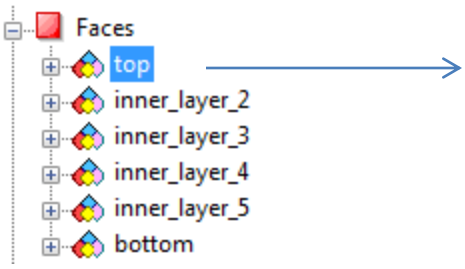
Bottom

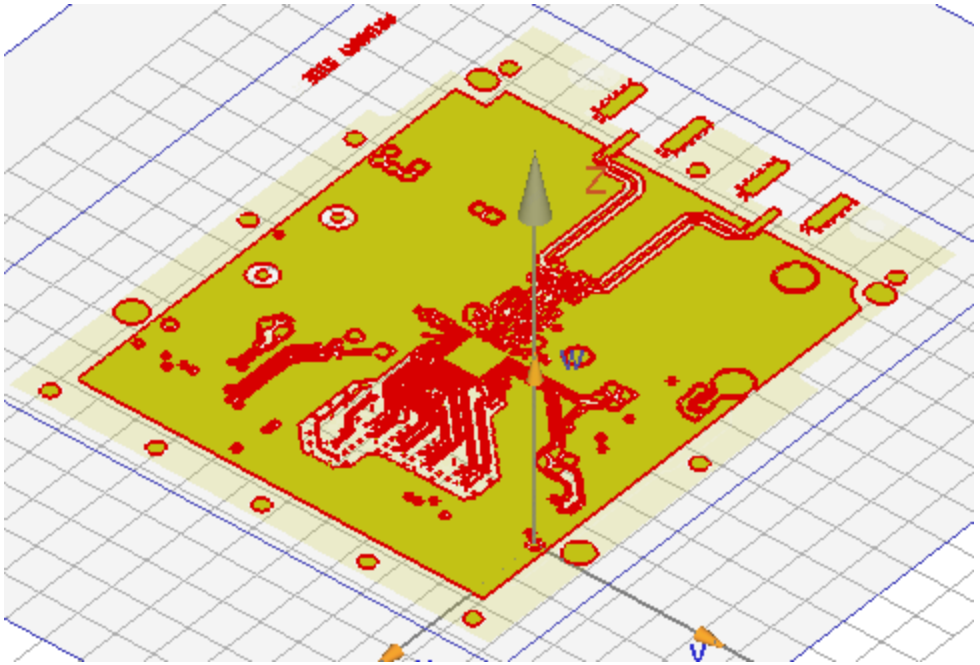
6 PCB layers

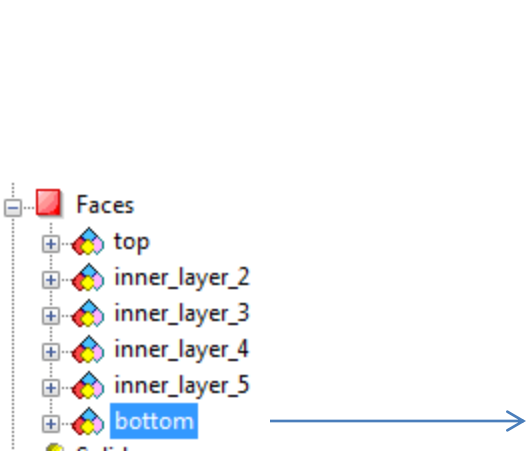


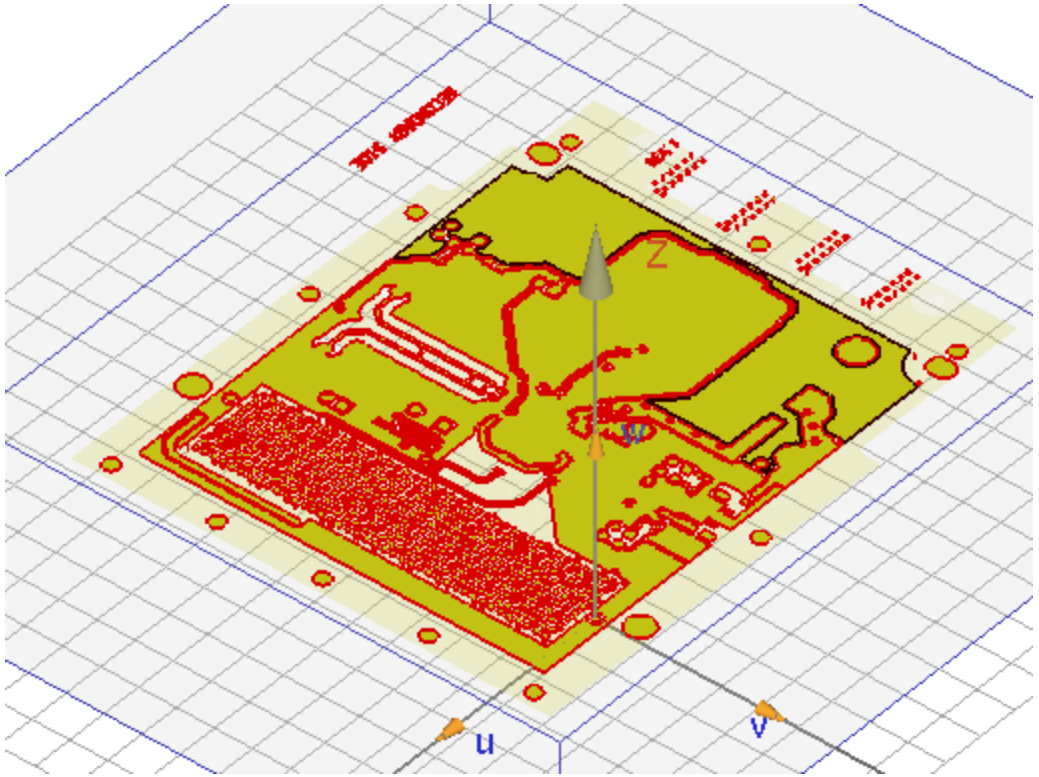


User can select each face component to check the model layer by layer



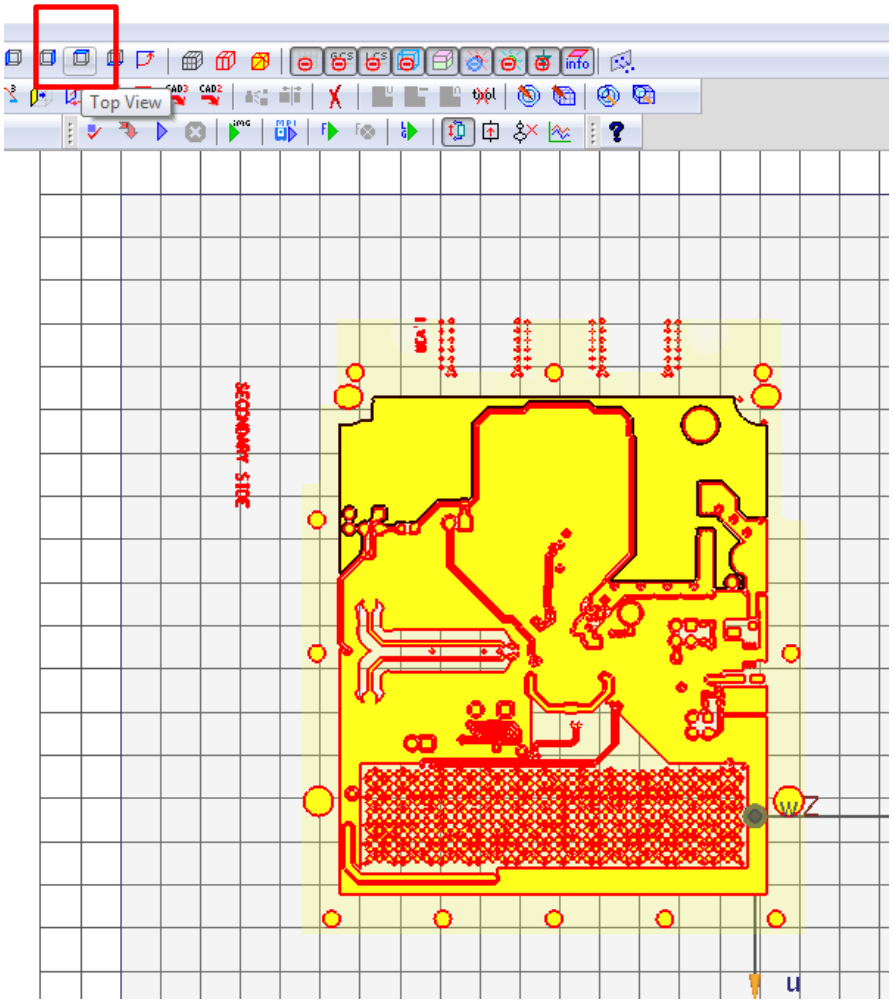



Faces
top
inner_layer_2
inner_layer_3
inner_layer_4
inner_layer_5
bottom

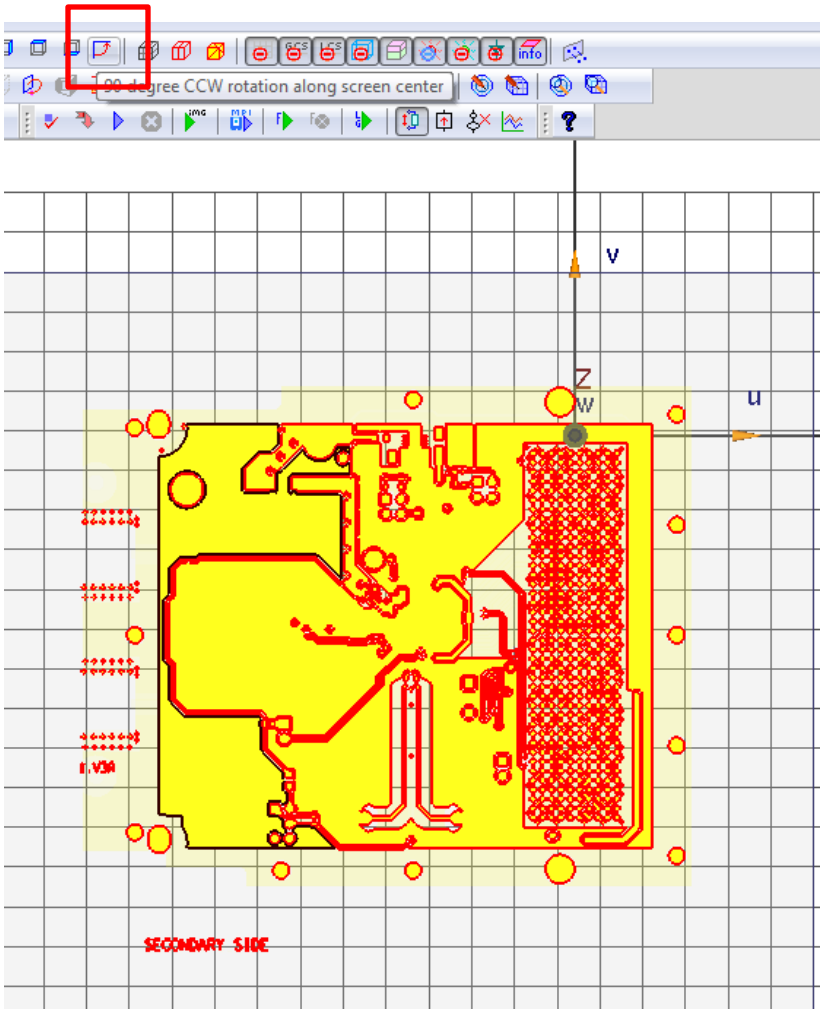

Z
u
v

If user want to see the model more clear,

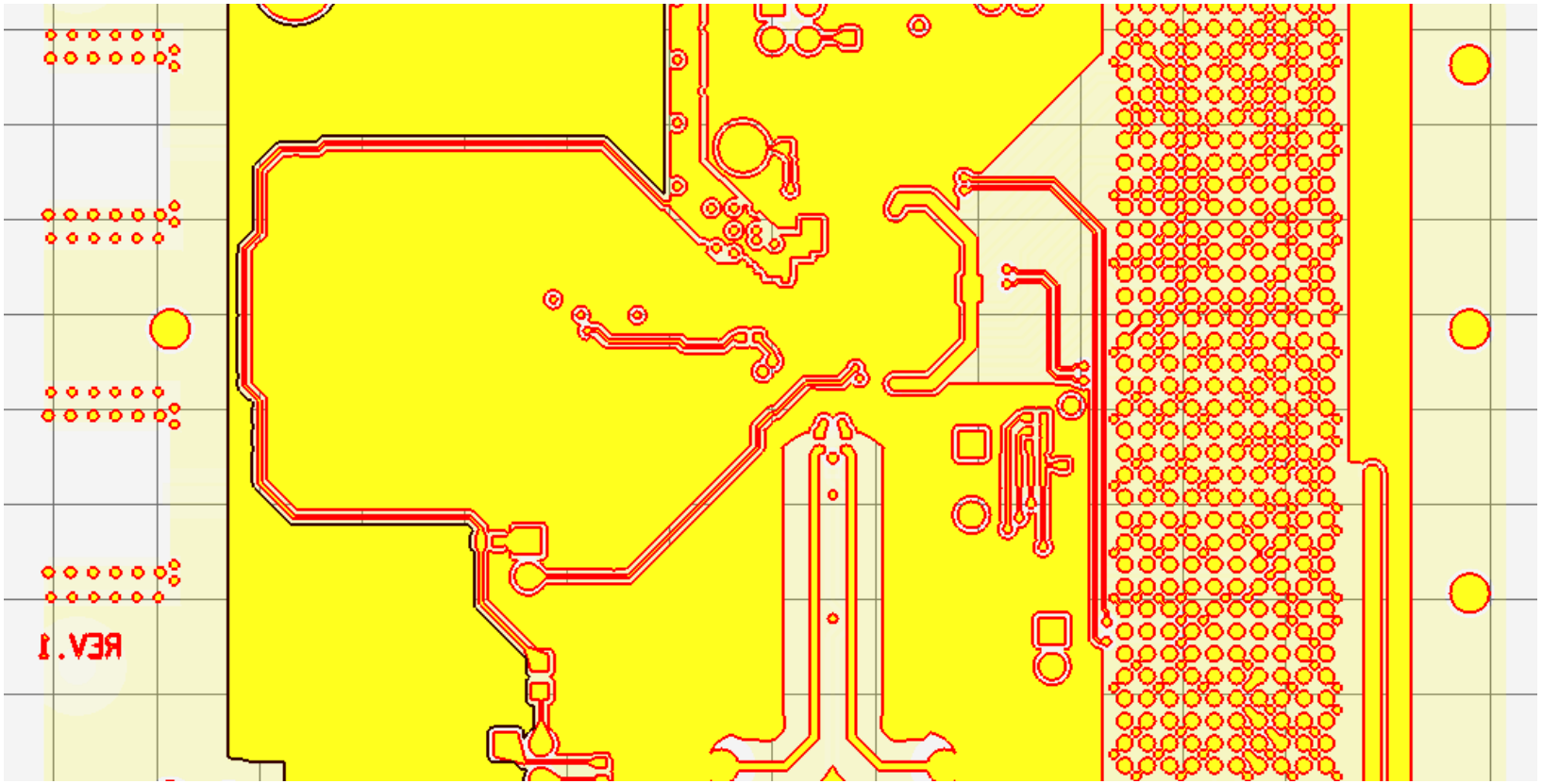
Top view



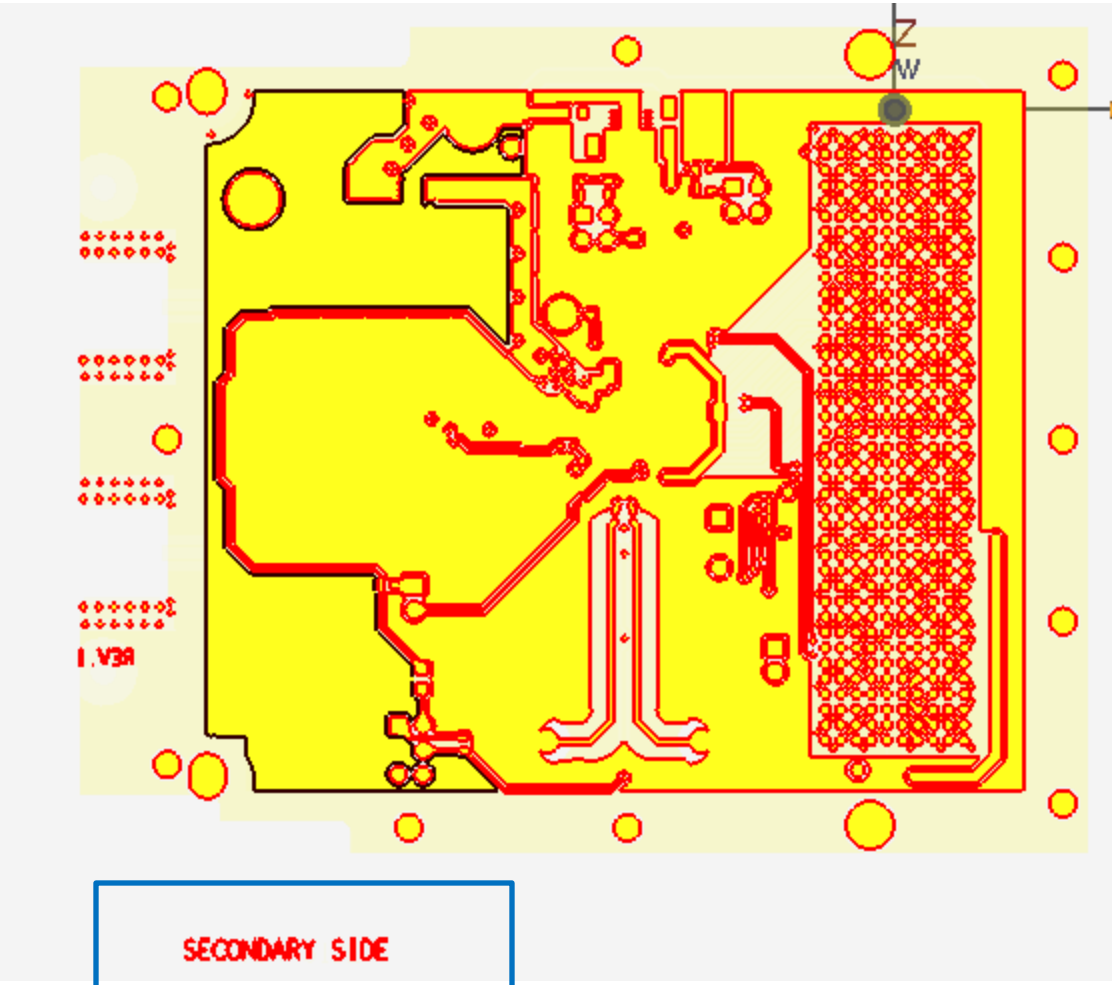
2D 90º rotation



Zoom by scrolling the mouse

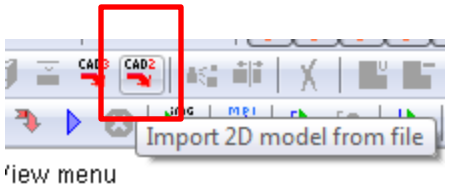


Optional 5.x, remove unnecessary shapes from model

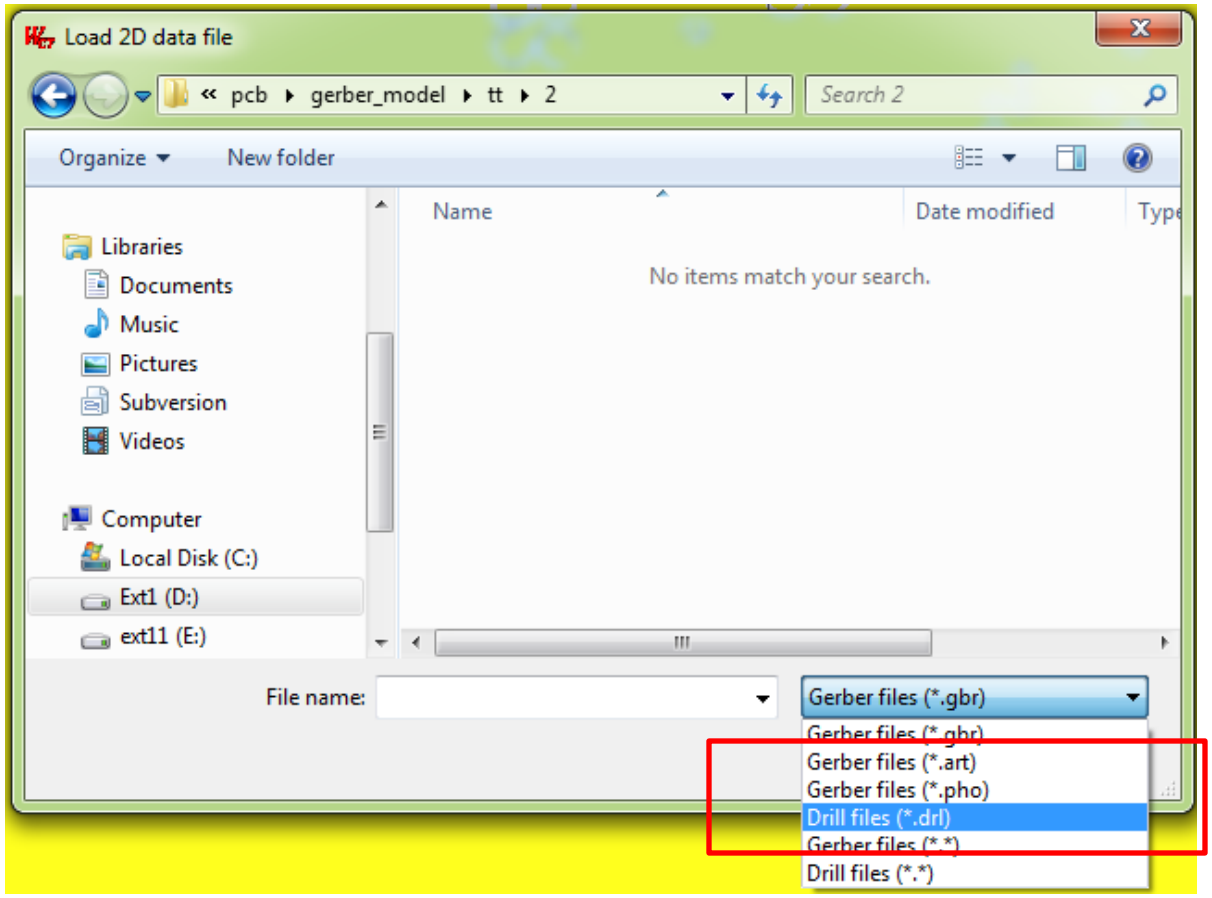


These components are for displaying purpose only, not real models, user can remove them from the project

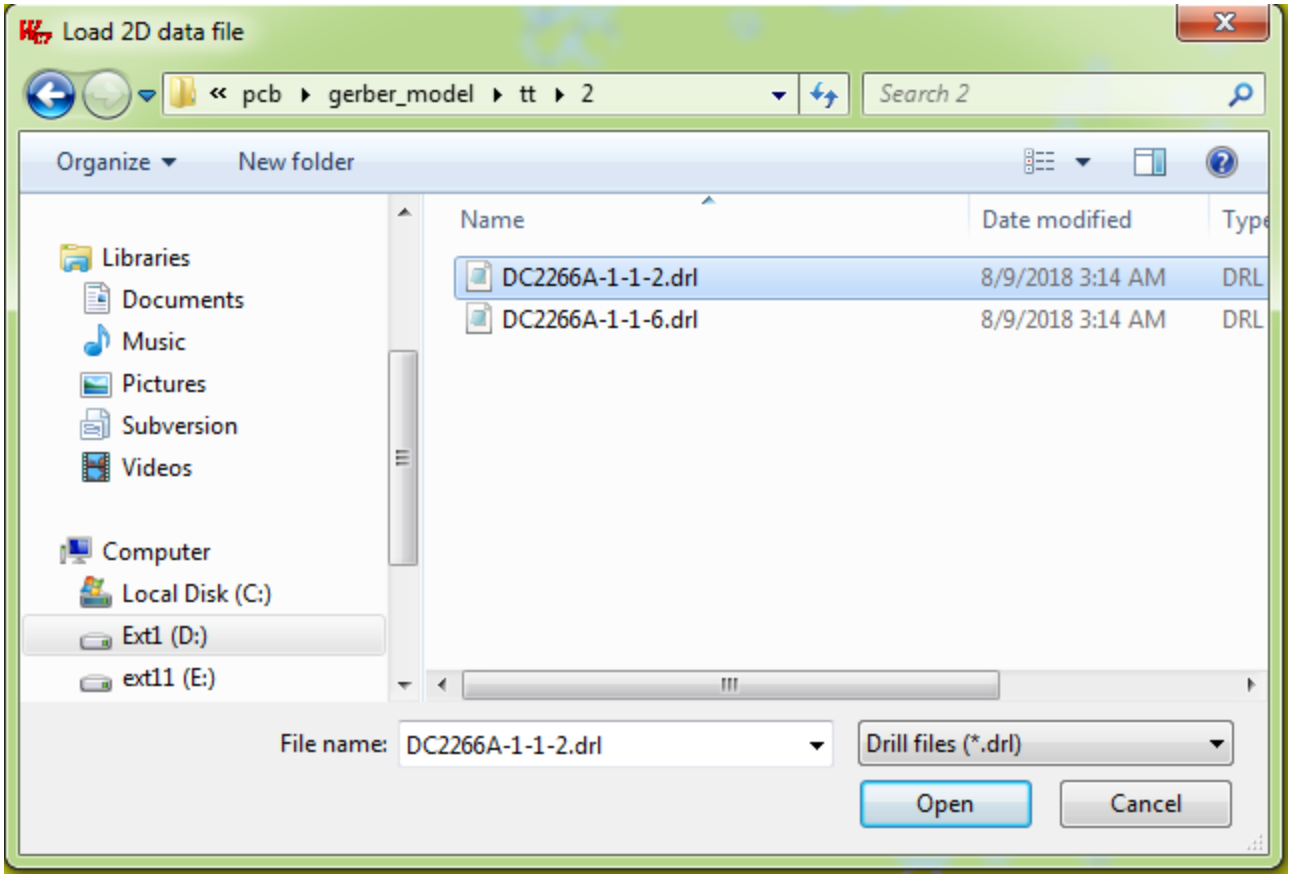
6. Import drill holes



'iew menu

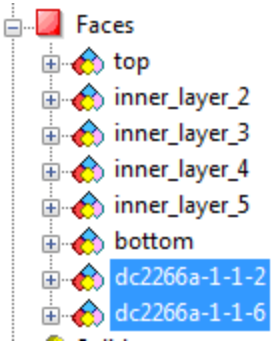


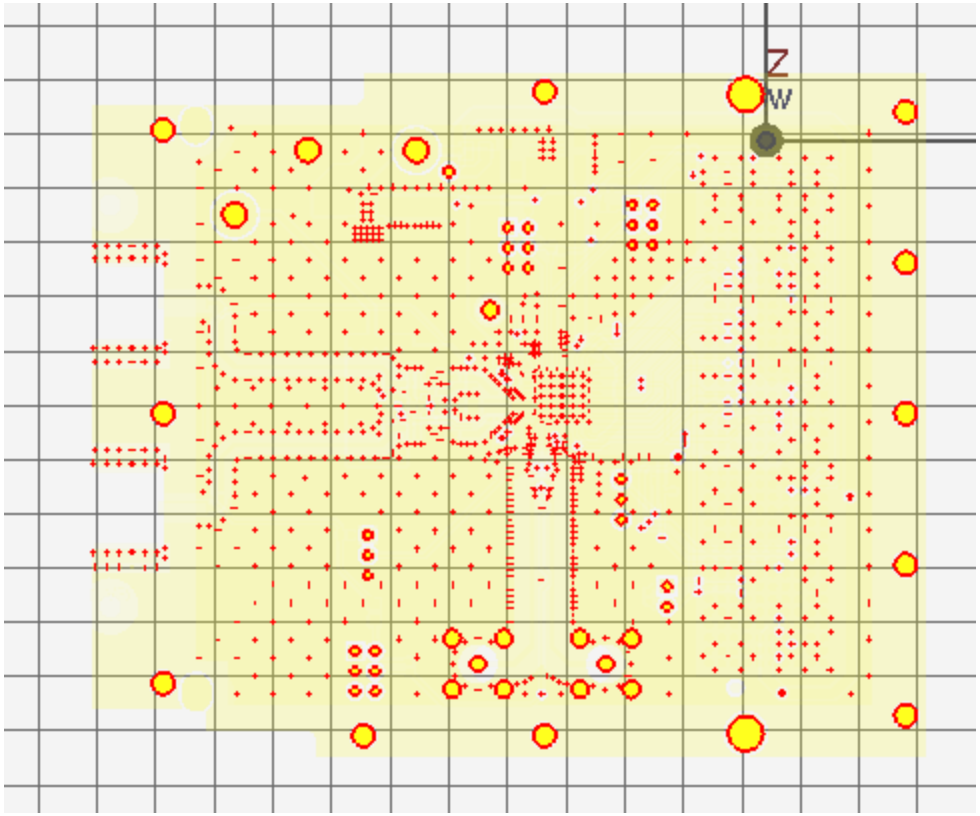
the drill files in this case have a suffix as "**drl**"


Load 2D data file
« pcb ▸ gerber_model ▸ tt ▸ 2
Search 2
Organize
New folder
Libraries
Documents
Music
Pictures
Subversion
Videos
Computer
Local Disk (C:)
Ext1 (D:)
ext11 (E:)
Name
Date modified
Type
DC2266A-1-1-2.drl
8/9/2018 3:14 AM
DRL
DC2266A-1-1-6.drl
8/9/2018 3:14 AM
DRL
File name:
DC2266A-1-1-2.drl
Drill files (*.drl)
Open
Cancel

After two drill files are loaded

Check the hole models





Note: the drilling hole will be defined as 2D planar faces in loading. User can convert them to PEC via by “Thicken” function after loading.

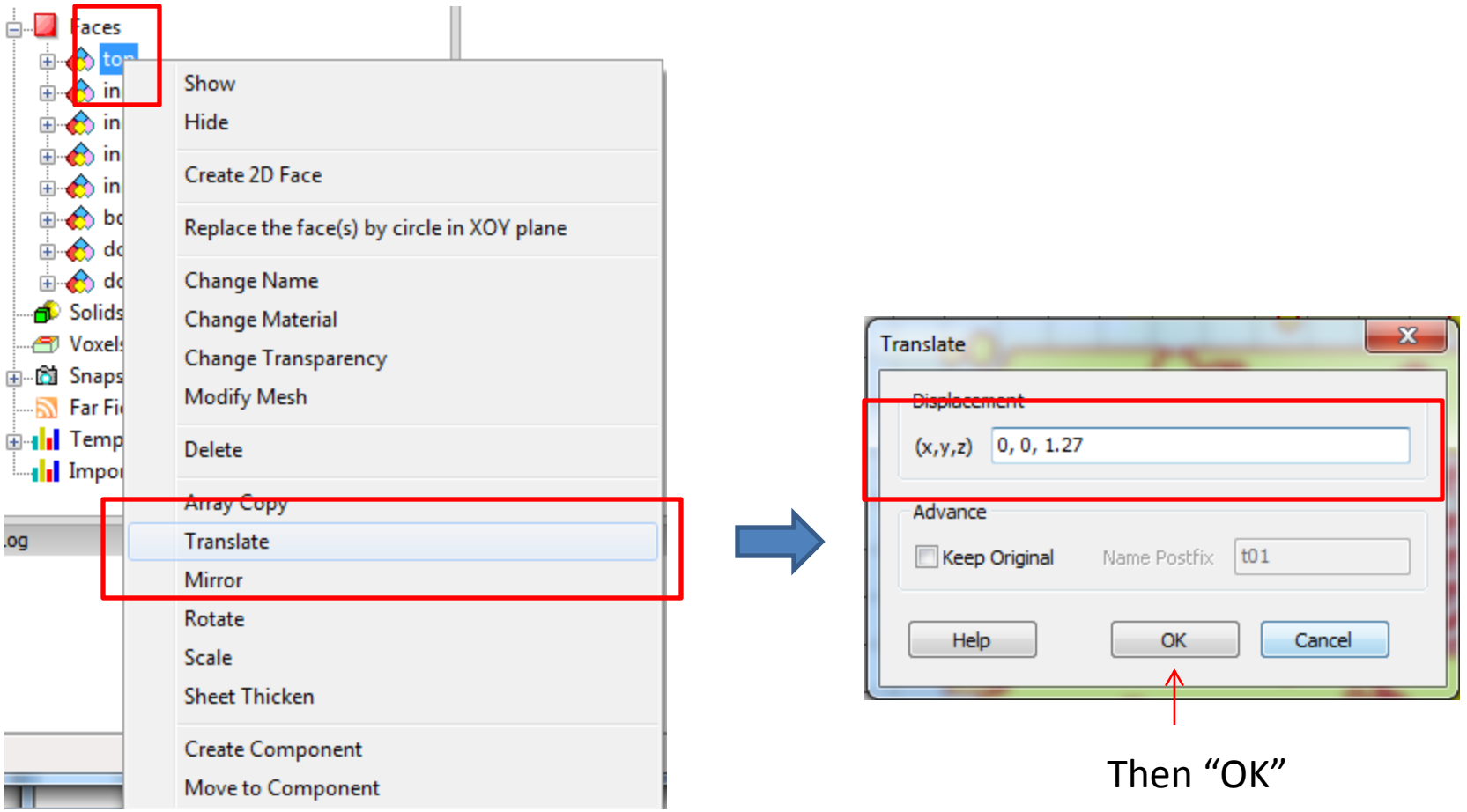
7. Shift each layer to the correct Z positions

Layer #	Color	Layer Icon	Layer Name	Thickness(...	Material	Conductivity(S...	Fill-in Dielectric	Er	Loss Tangent
1			Signal$Top	0.03429		5.8e+007		[1]	[0]
			Medium$Dielectric1	0.254		0		4.3	0
2			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric3	0.254		0		4.3	0
3			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric5	0.254		0		4.3	0
4			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric7	0.254		0		4.3	0
5			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric9	0.254		0		4.3	0
6			Signal$Bottom	0.03429		5.8e+007		[1]	[0]

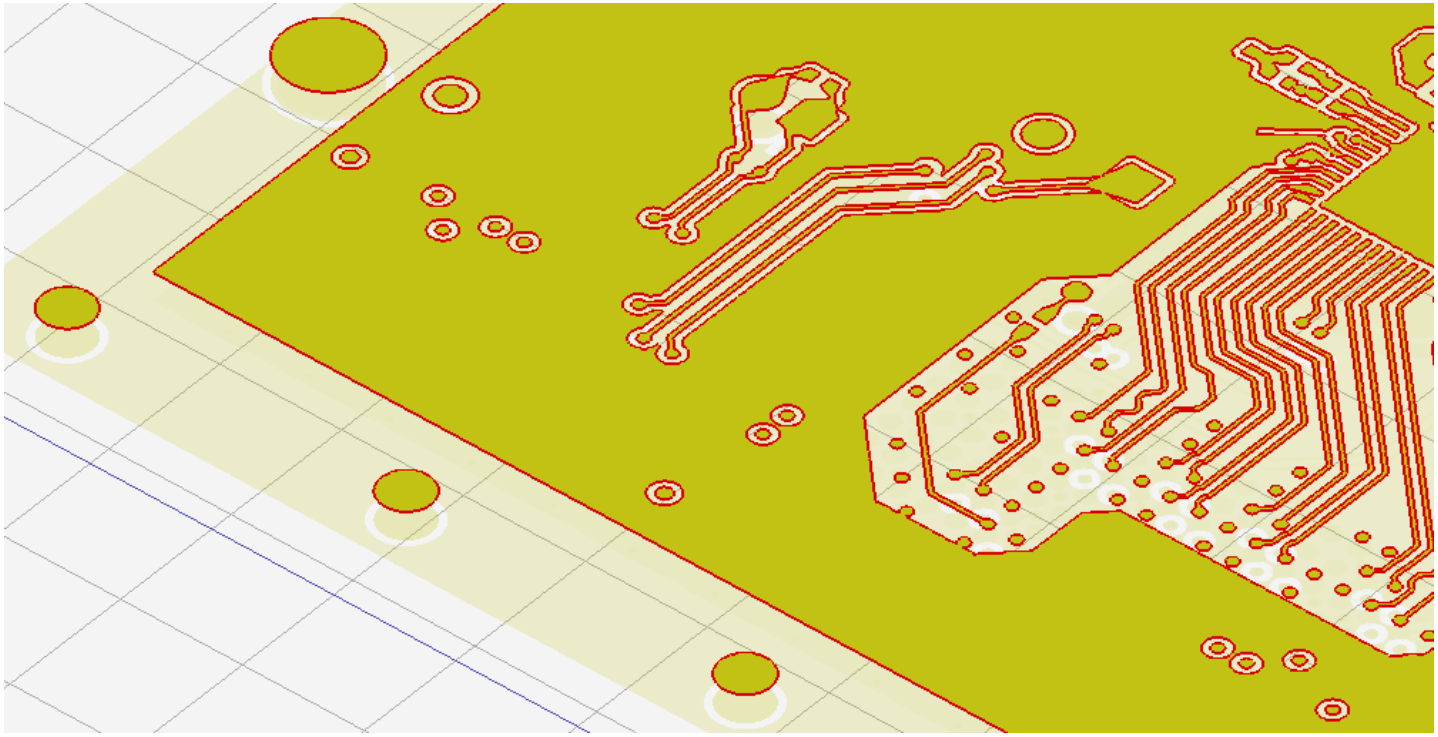
Based on the table, if we define the bottom layer has Z=0, other layers will be at:

Top: 0.254*5 = 1.27
2nd layer: 0.254*4 = 1.016
3rd layer: 0.254*3 = 0.762
4th layer: 0.254*2 = 0.508
5th layer: 0.254*1 = 0.254
Bottom: 0

For example, shift the ***top*** layer to Z=1.27 mm

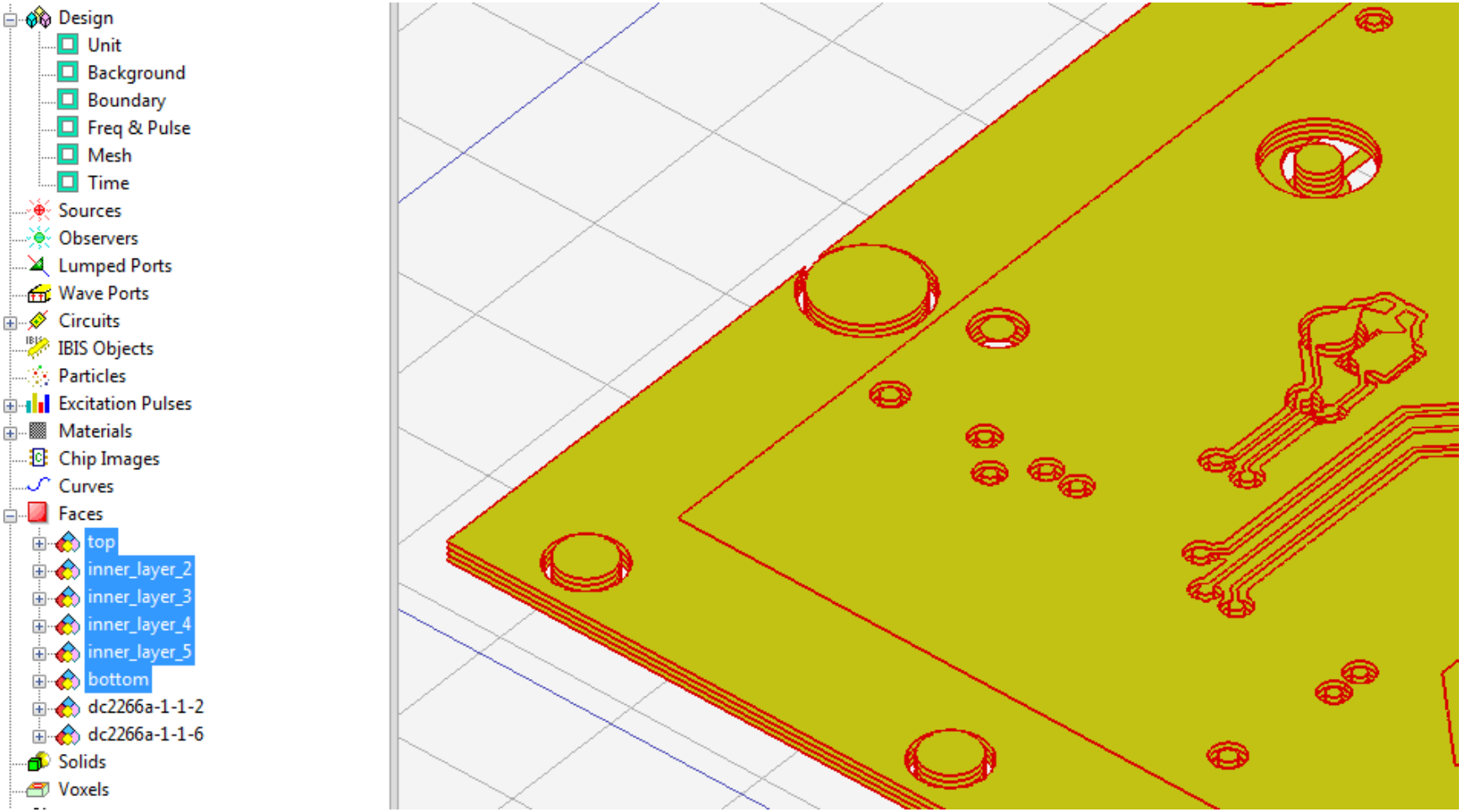


The top layer has been shifted to Z=1.27 mm



Repeat this procedure for other layers to shift them to the correct Z positions

The following figure shows the shifted models



Layer #	Color	Layer Icon	Layer Name	Thickness(...	Material	Conductivity(S...	Fill-in Dielectric	Er	Loss Tangent
1			Signal$Top	0.03429		5.8e+007		[1]	[0]
			Medium$Dielectric1	0.254		0		4.3	0
2			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric3	0.254		0		4.3	0
3			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric5	0.254		0		4.3	0
4			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric7	0.254		0		4.3	0
5			Signal$Inner_La...	0.03429		5.8e+007		[4.3]	[0]
			Medium$Dielectric9	0.254		0		4.3	0
6			Signal$Bottom	0.03429		5.8e+007		[1]	[0]

Note:

In reality, each PCB layer should have a thickness of 0.03439 mm based on the table. However, this thin thickness will cause very fine mesh in the FDTD engine, makes the simulation Δt become very small and the number of simulation steps become huge.

According to our experience, using a 0-thickness PEC face to represent the thin PEC object will not affect the simulation result significantly, but the mesh will be much coarser and the simulation Δt will become much larger compared to the fine mesh setting, it will significantly reduce the simulation time.

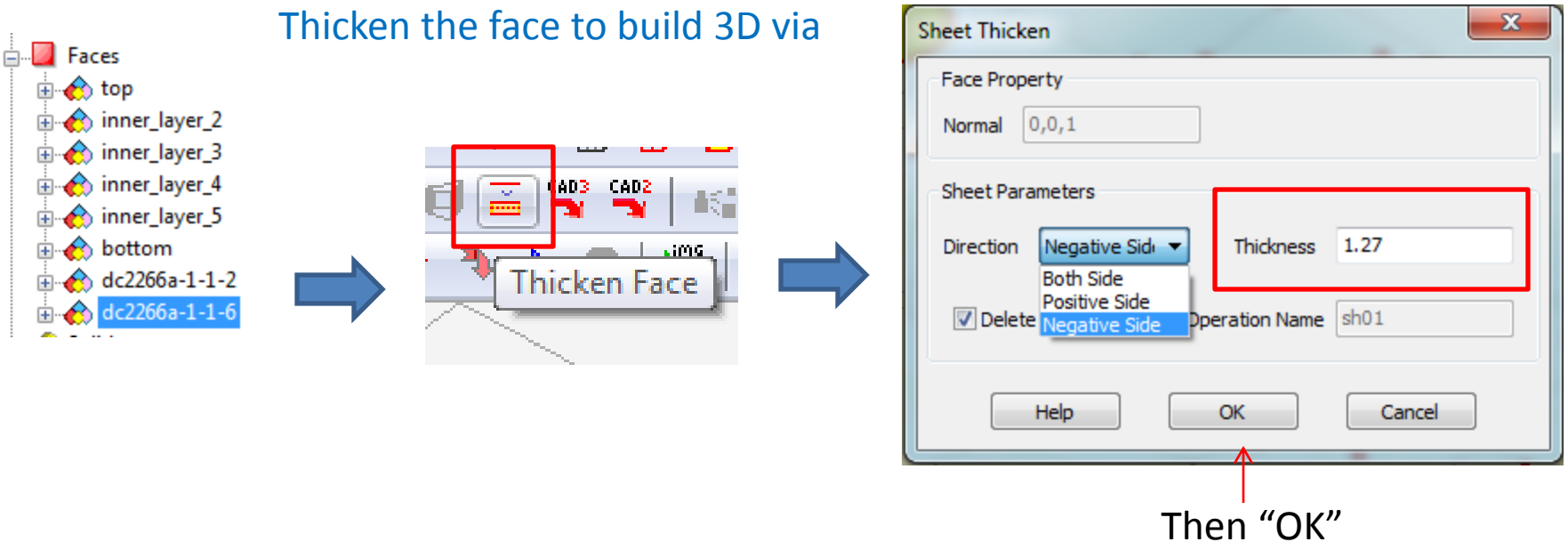
So, in a PCB simulation, we suggest to use 2D planar faces to represent PCB models. If user want to get a very accurate simulation result, he can also change these 2D planar faces to thin 3D models by "Thicken" function in Wavenology EM GUI.

8. Convert the drill hole to PEC via

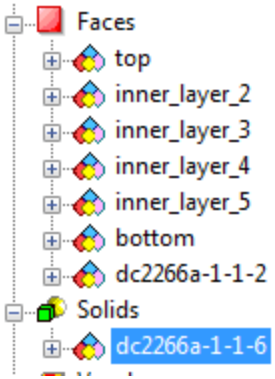
Based on the drill file name, we know the component “1-2” means that this hole model will be the via connecting layer top & 2nd layer; the component “1-6” means that this model will be the via go through the top layer and the bottom layer.

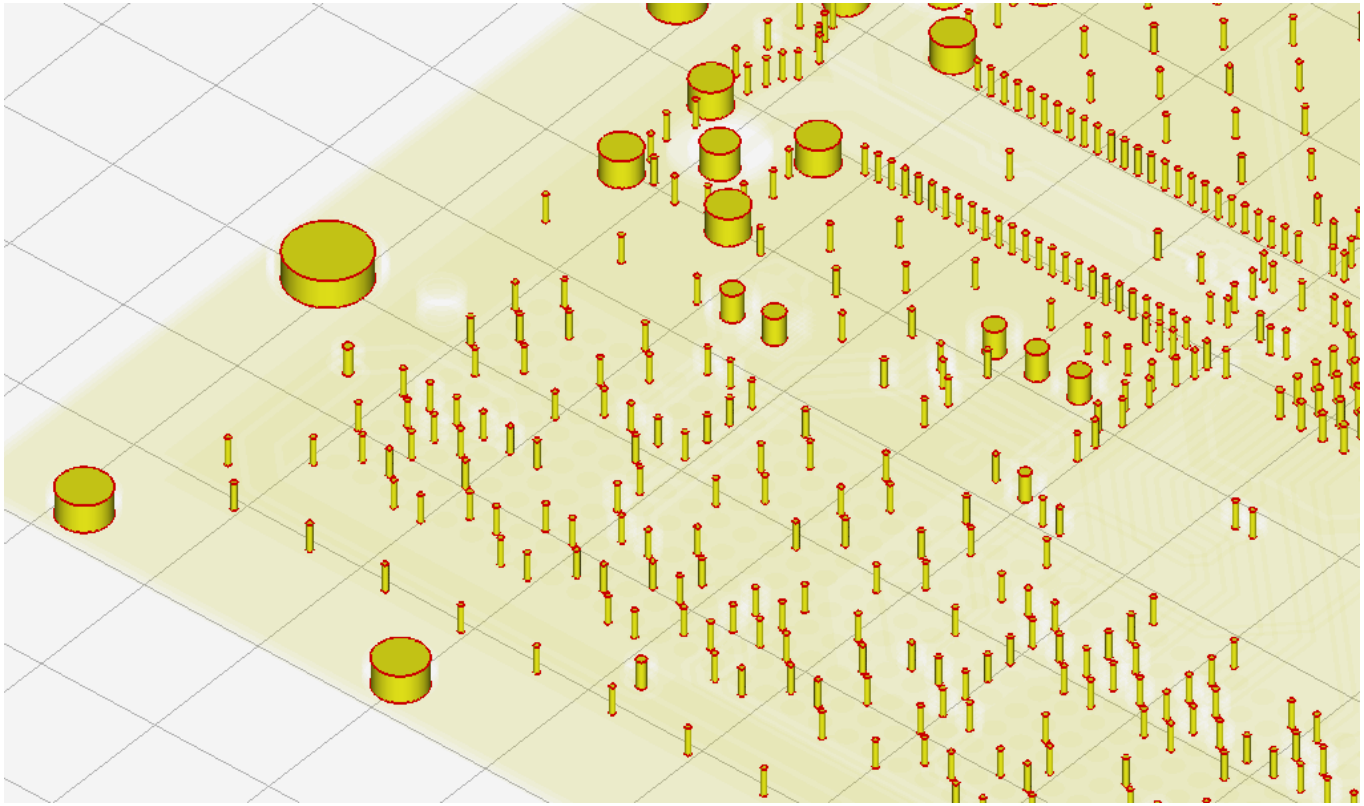
a) So, we shift all drill components to Z=1.27 mm to make them aligned to the top layer in the 1st step.

b) Then, convert all elements in the drill component “**1-6**” to 3D via with a height of 1.27mm by “Thicken” function.



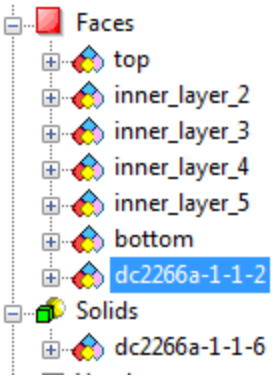
After conversion, the via model goes through top & bottom layer is as following

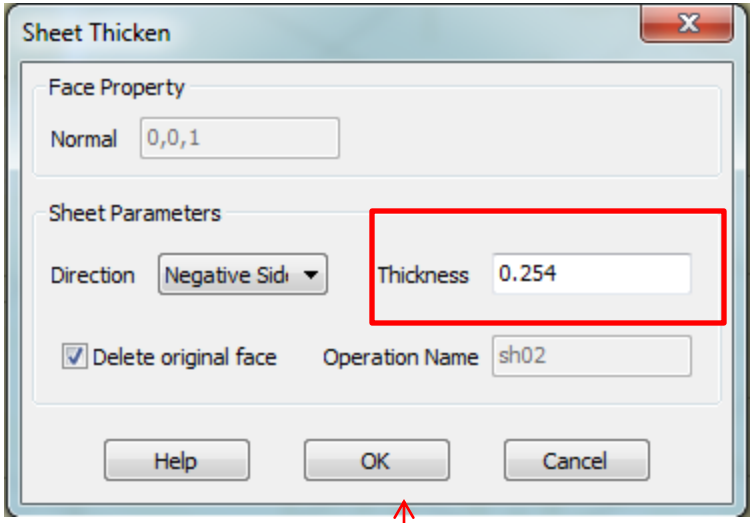




Then, convert all elements in the drill component “1-2” to via with a height of 0.254 mm.

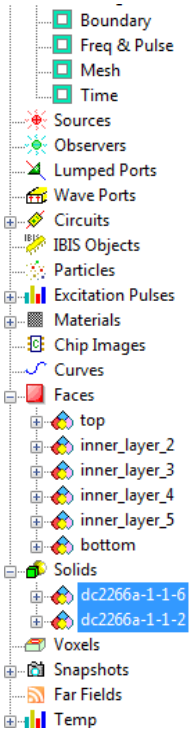
Thicken the face to build 3D via

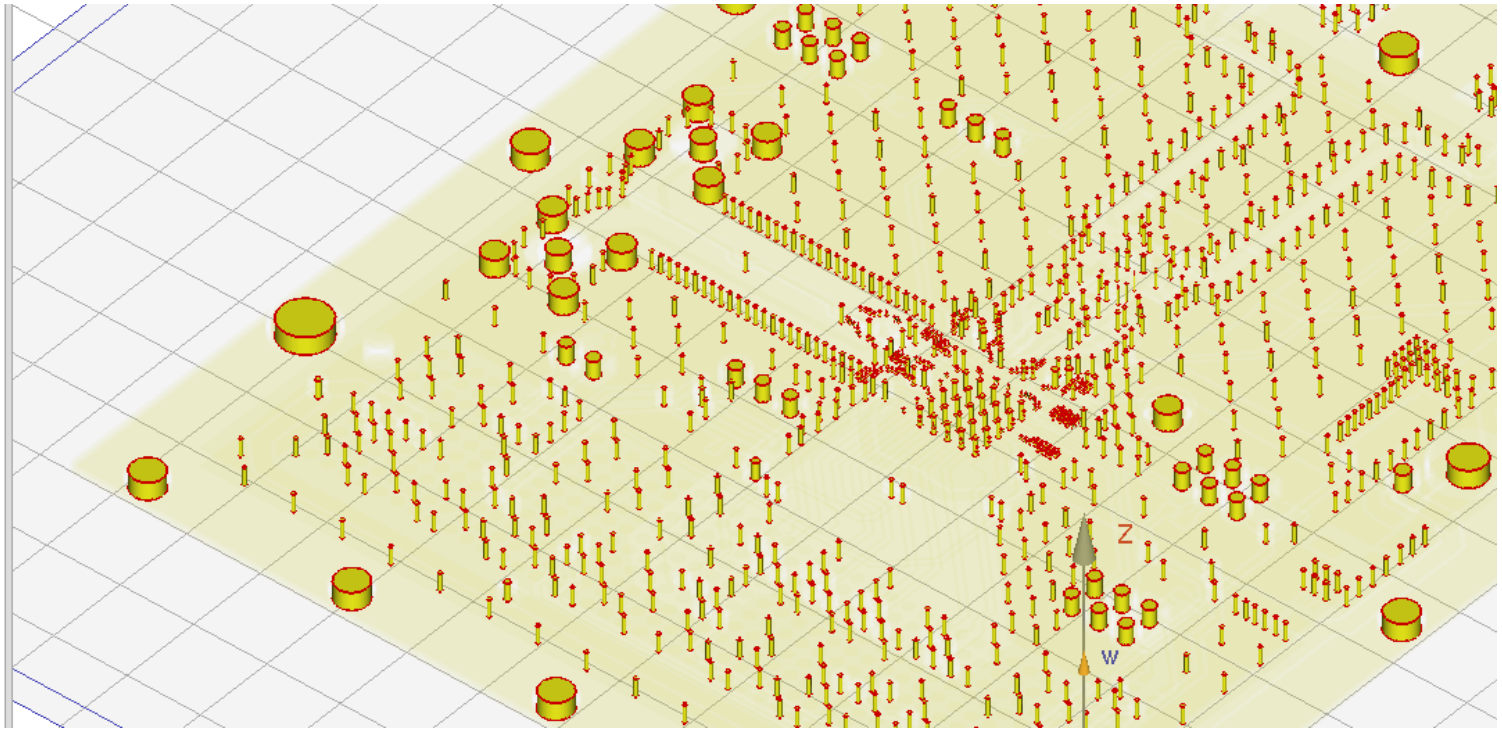




Then “OK”

After all via are built, the models are shown as the following figure





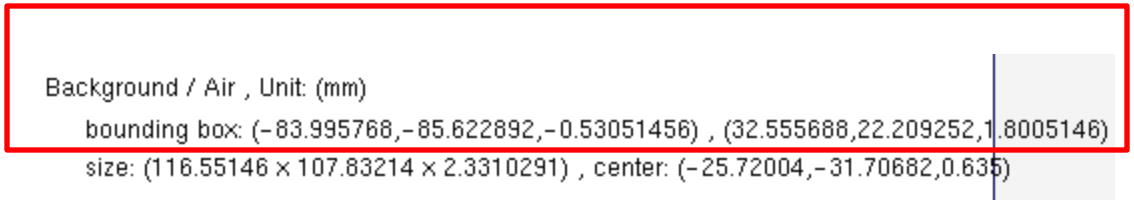
9. Build substrate layers

From the table in step 7, if we define the bottom layer is at Z=0, the Z coordinates range of each substrate layer will be,

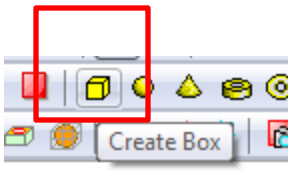
Top: 0.254*5 = 1.27
2nd layer: 0.254*4 = 1.016
3rd layer: 0.254*3 = 0.762
4th layer: 0.254*2 = 0.508
5th layer: 0.254*1 = 0.254
Bottom: 0

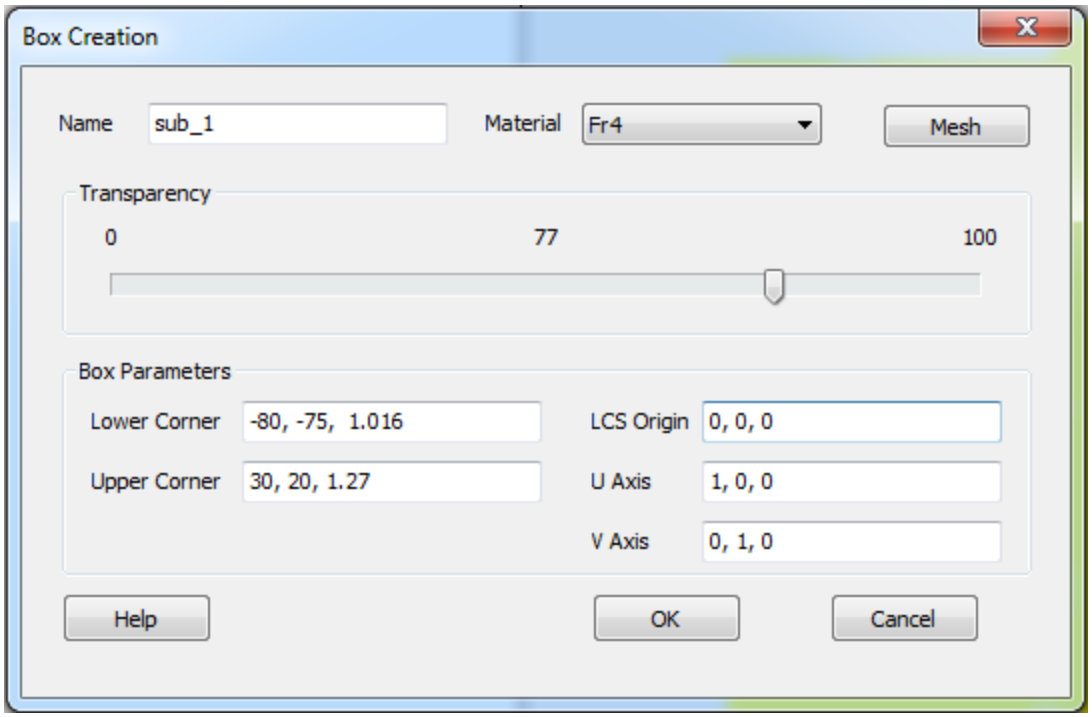
Substrate 1: z=1.016-1.27
Substrate 2: z=0.762-1.016
Substrate 3: z=0.508-0.762
Substrate 4: z=0.254-0.508
Substrate 5: z=0-0.254

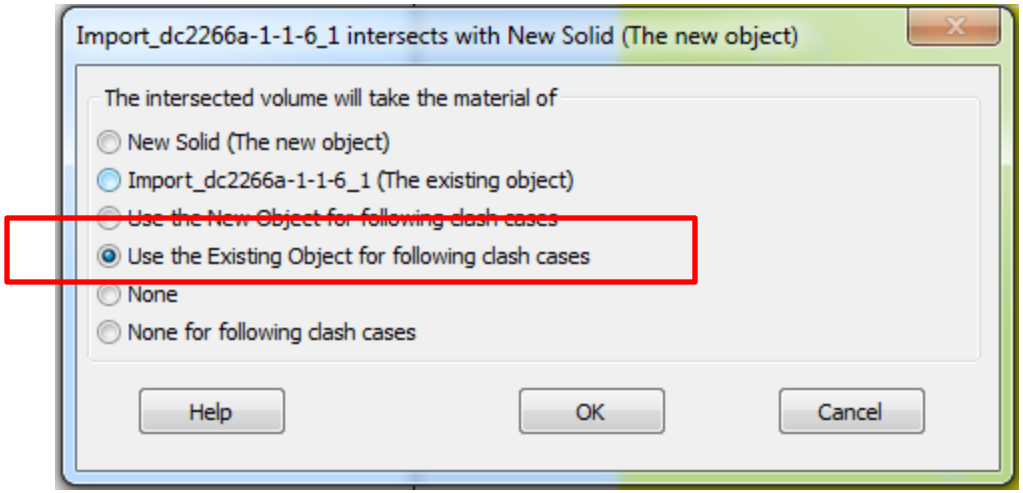
Based on the bounding box of whole models, we know that, the x & y range: (-84, -86) – (33, 22) can totally enclose all models with some gaps.



Create Substrate 1: z=1.016-1.27, x=-80-30, y=-75-20

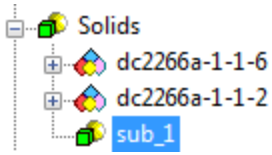


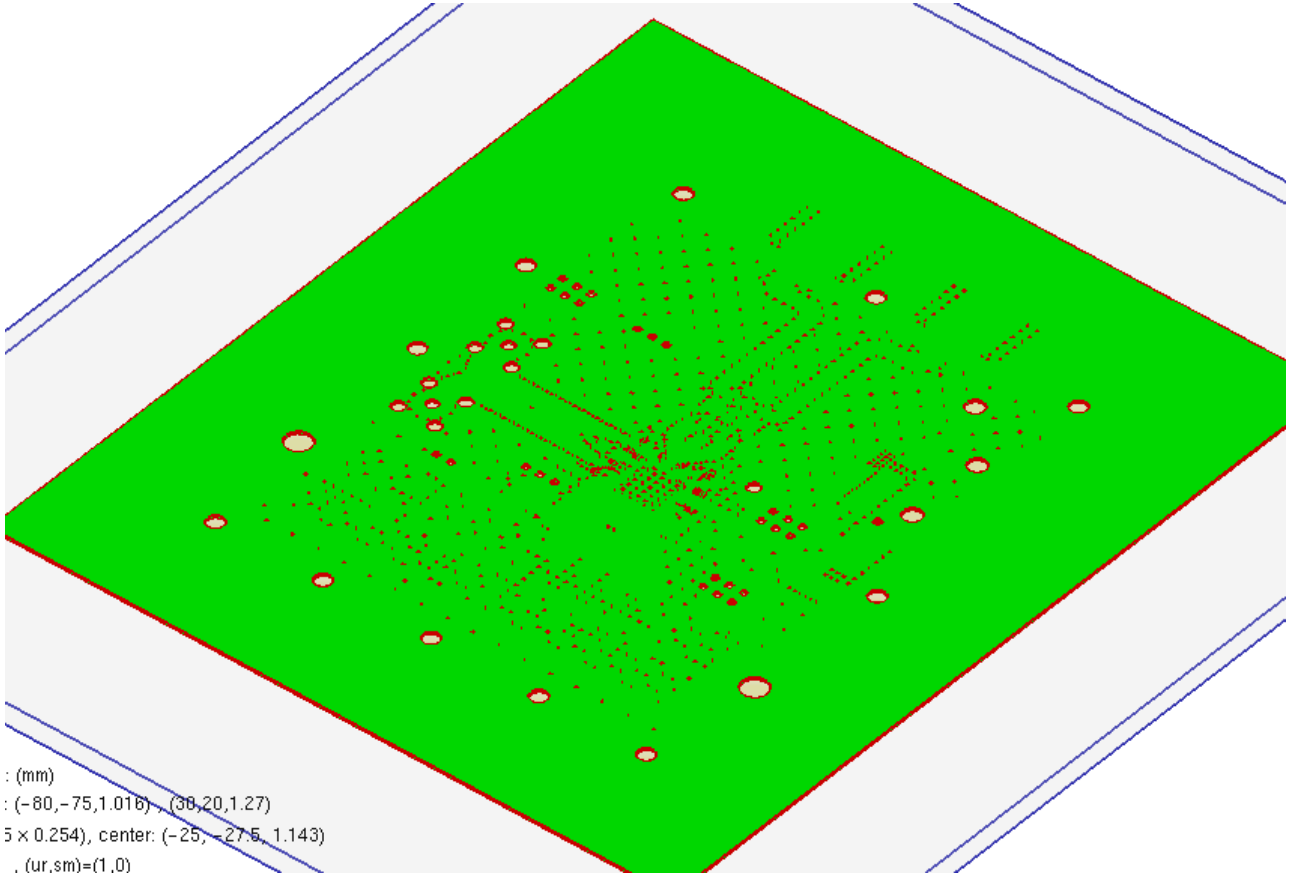




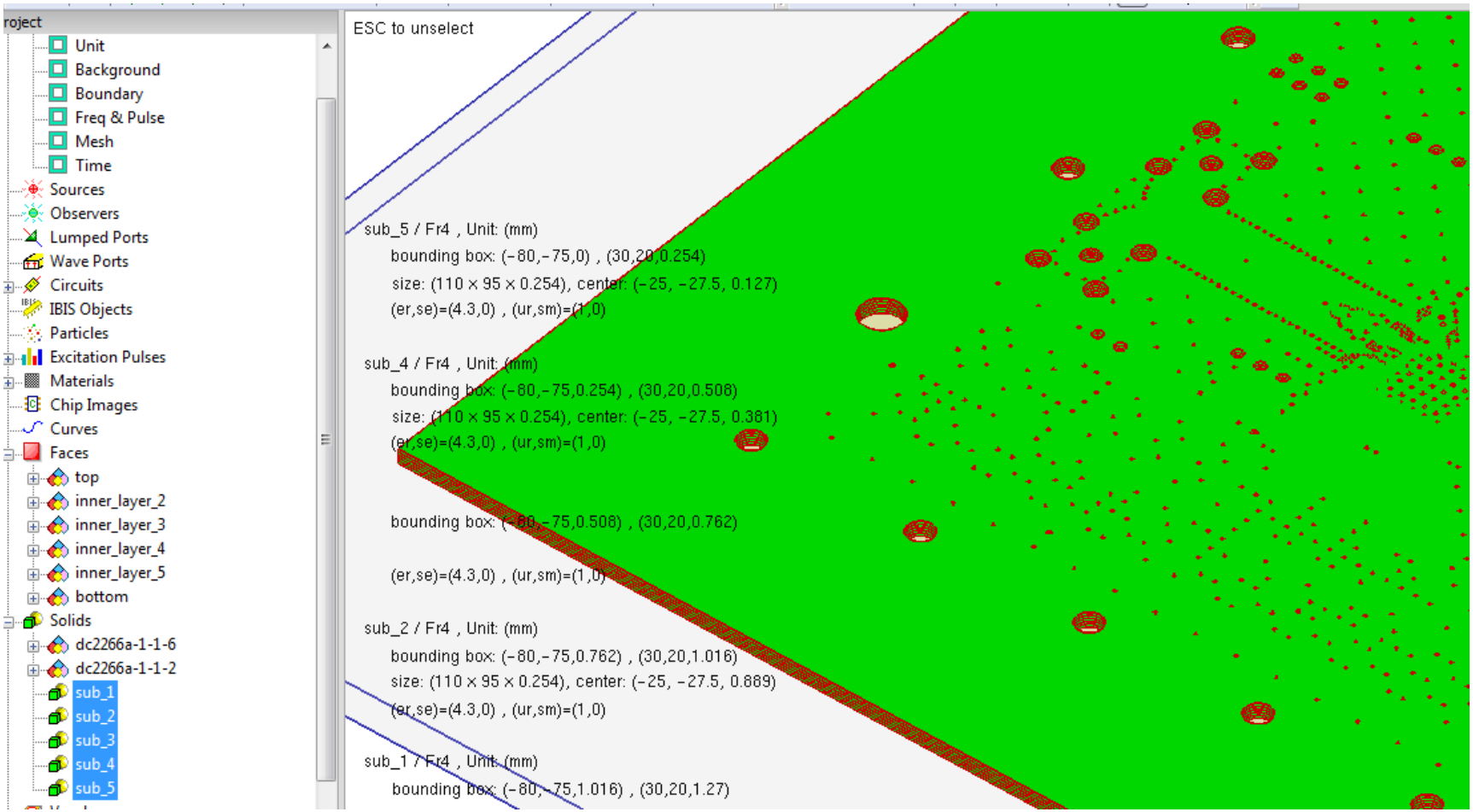
This substrate layer will clash with via in “1-2” and “1-6”, we will keep the via and make holes in this substrate, which equals to: (substrate – existing via)

After this layer is built

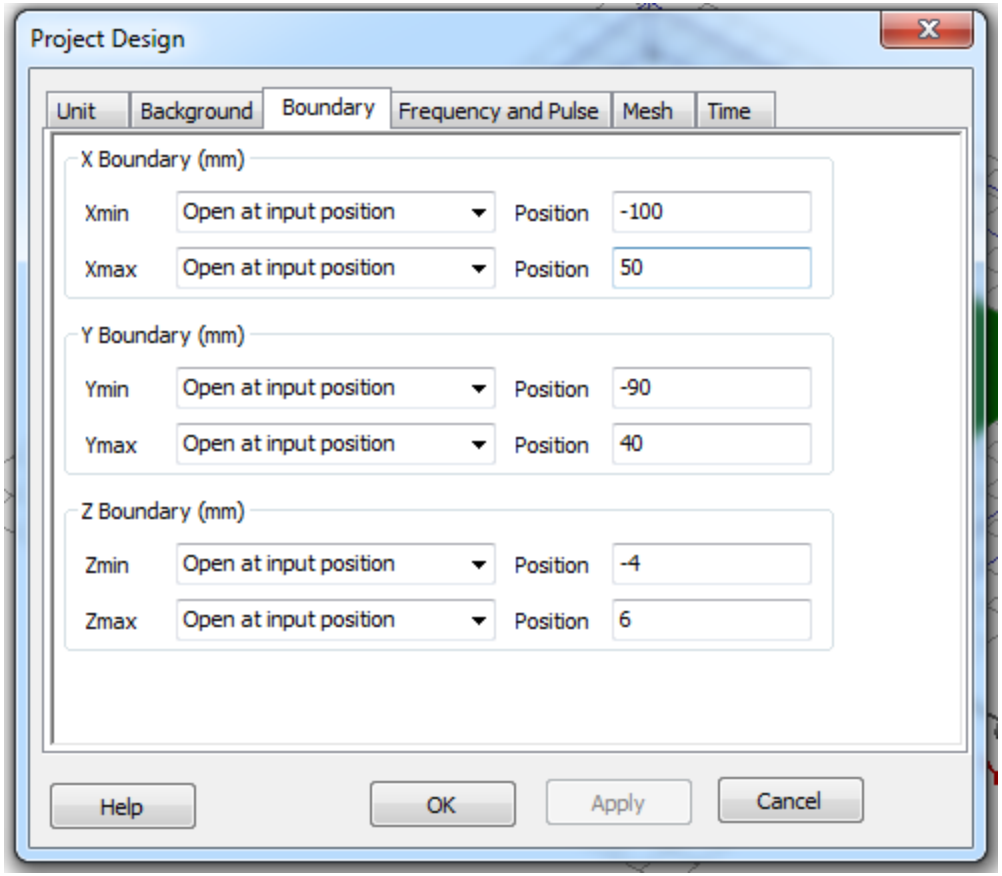




With the same procedure, we create Substrate 2, 3, 4 & 5, with the same X, Y range as **sub_1** and a correct Z range as listed in the beginning of step 9.

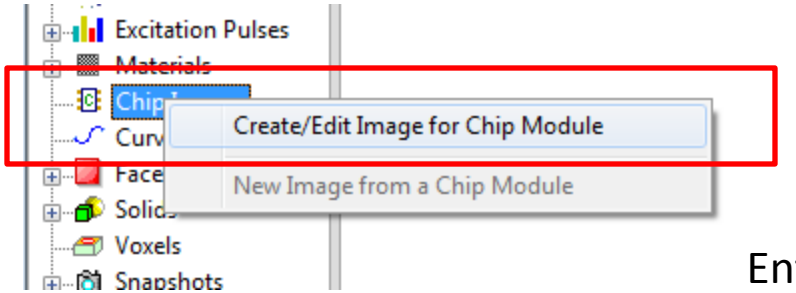


Optional 9.x, adjust the computational domain size to have a better ratio in "length vs. height"

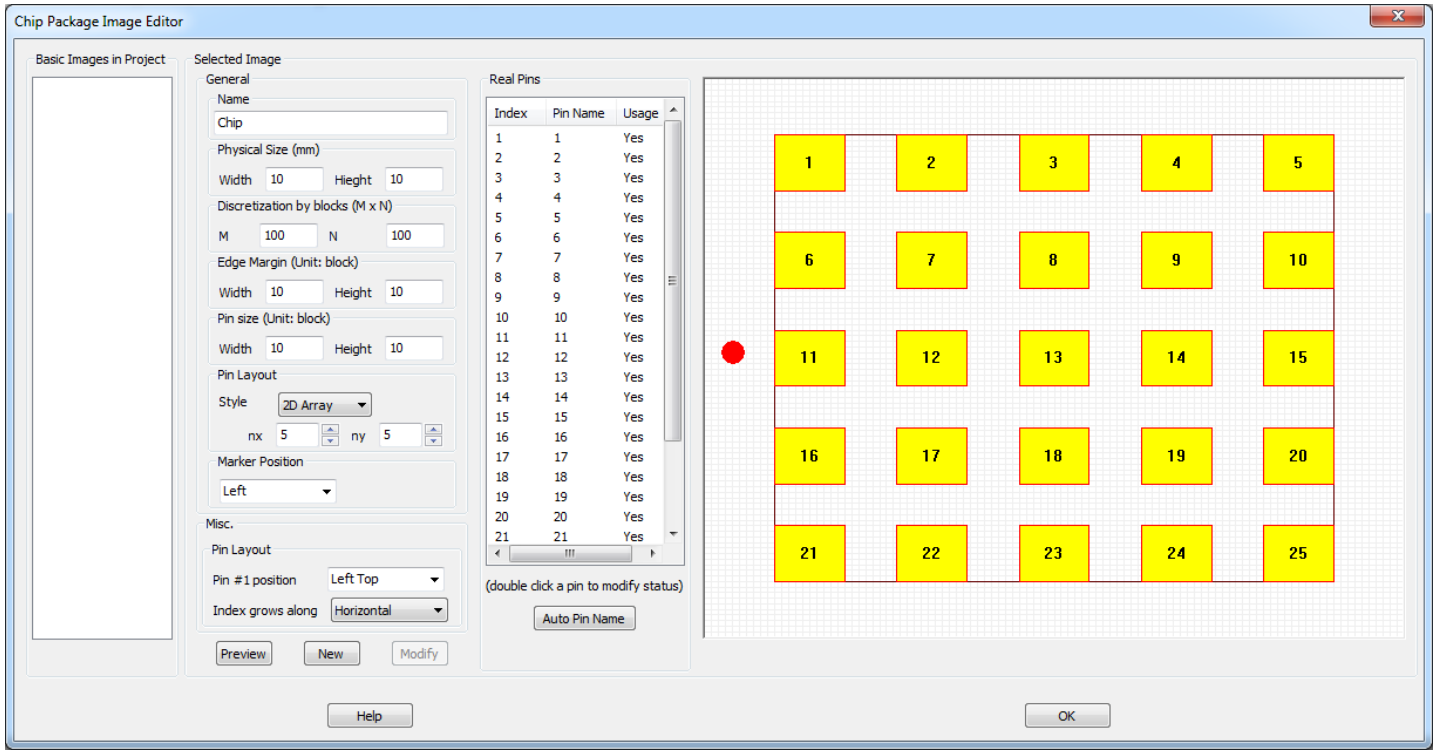


Optional 10, define an image for chip LTC2107 in the board to make the pads of chip more readable

Note: this step is not an essential step for the simulation, it will not affect the simulation result, just make the model more understandable.

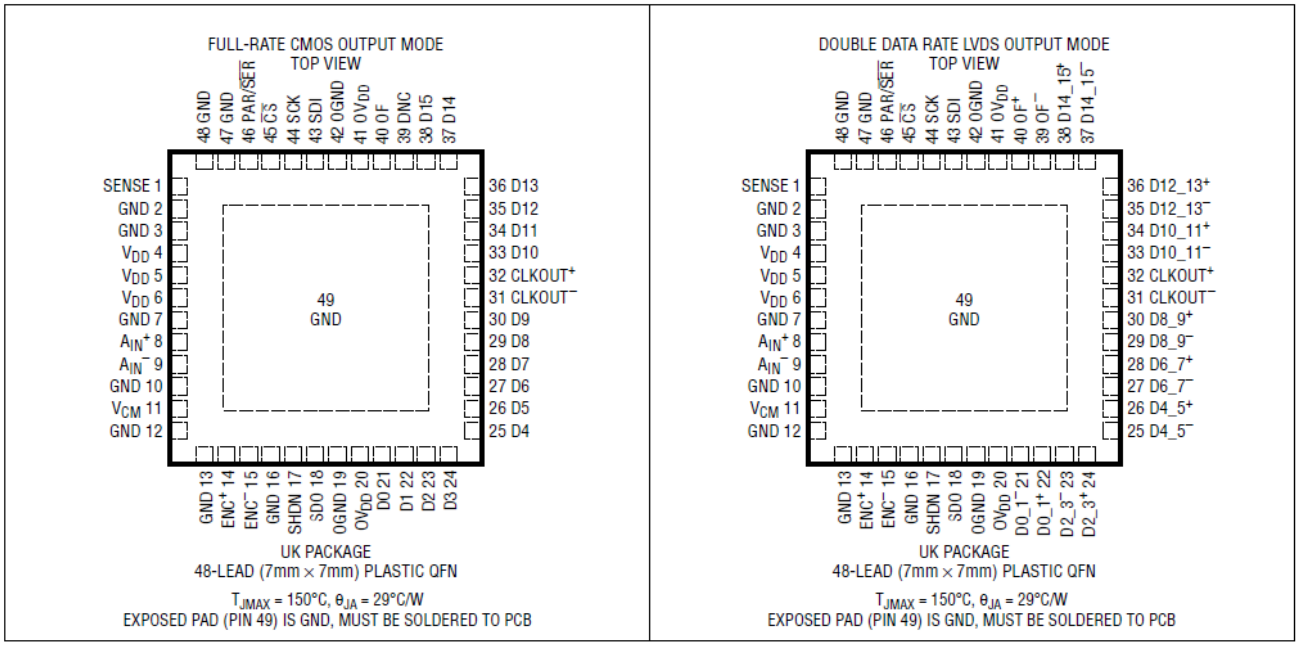


Enter the “Chip Package Image Editor”



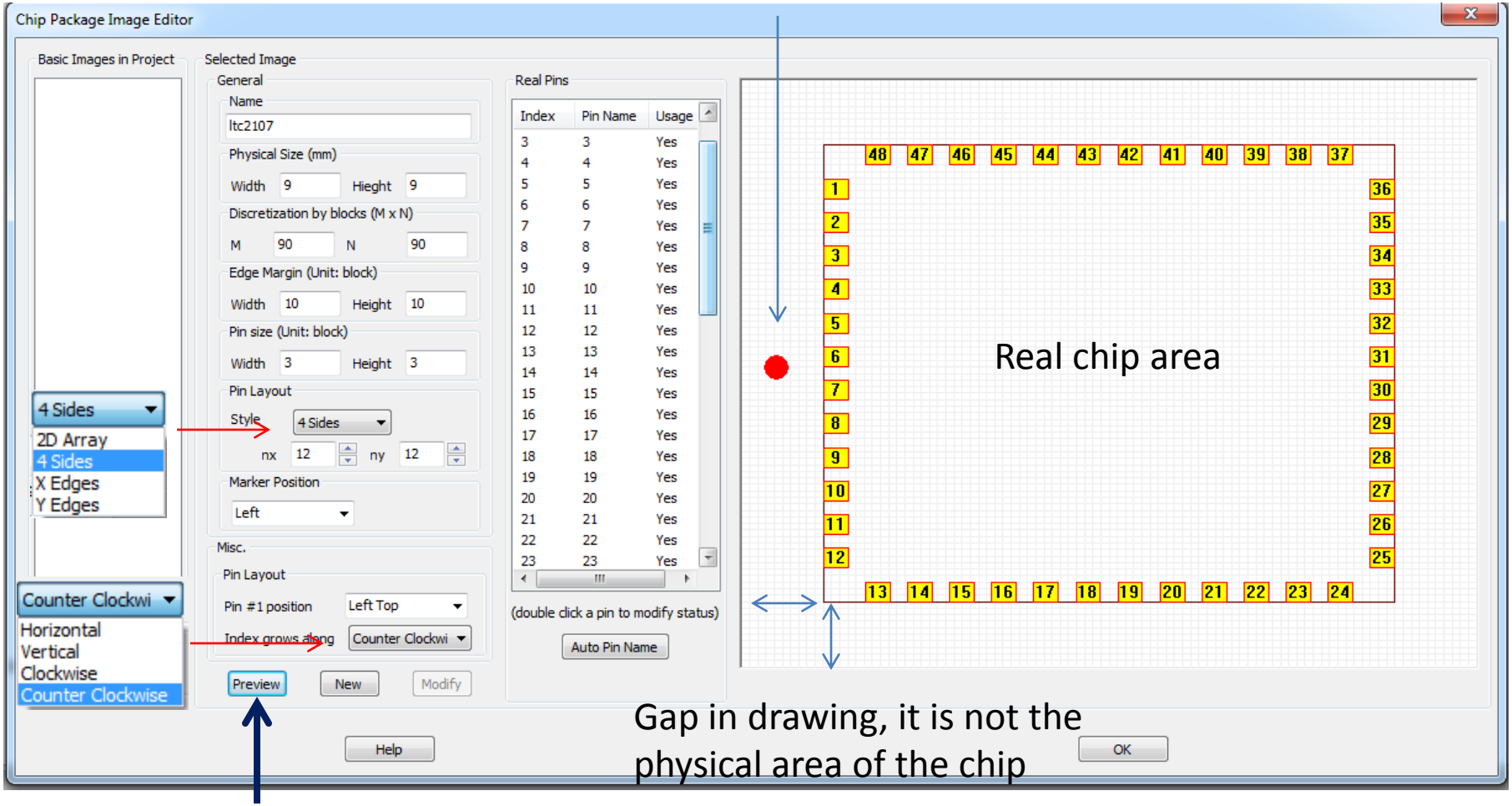
Based on the LTC2107 documentation, the size of chip is 7x7 mm^2, the layout of pin is as following, totally 49 pins. 48 pins are on the 4 edges.
- 48-Lead (7mm × 7mm) QFN Package

PIN CONFIGURATION



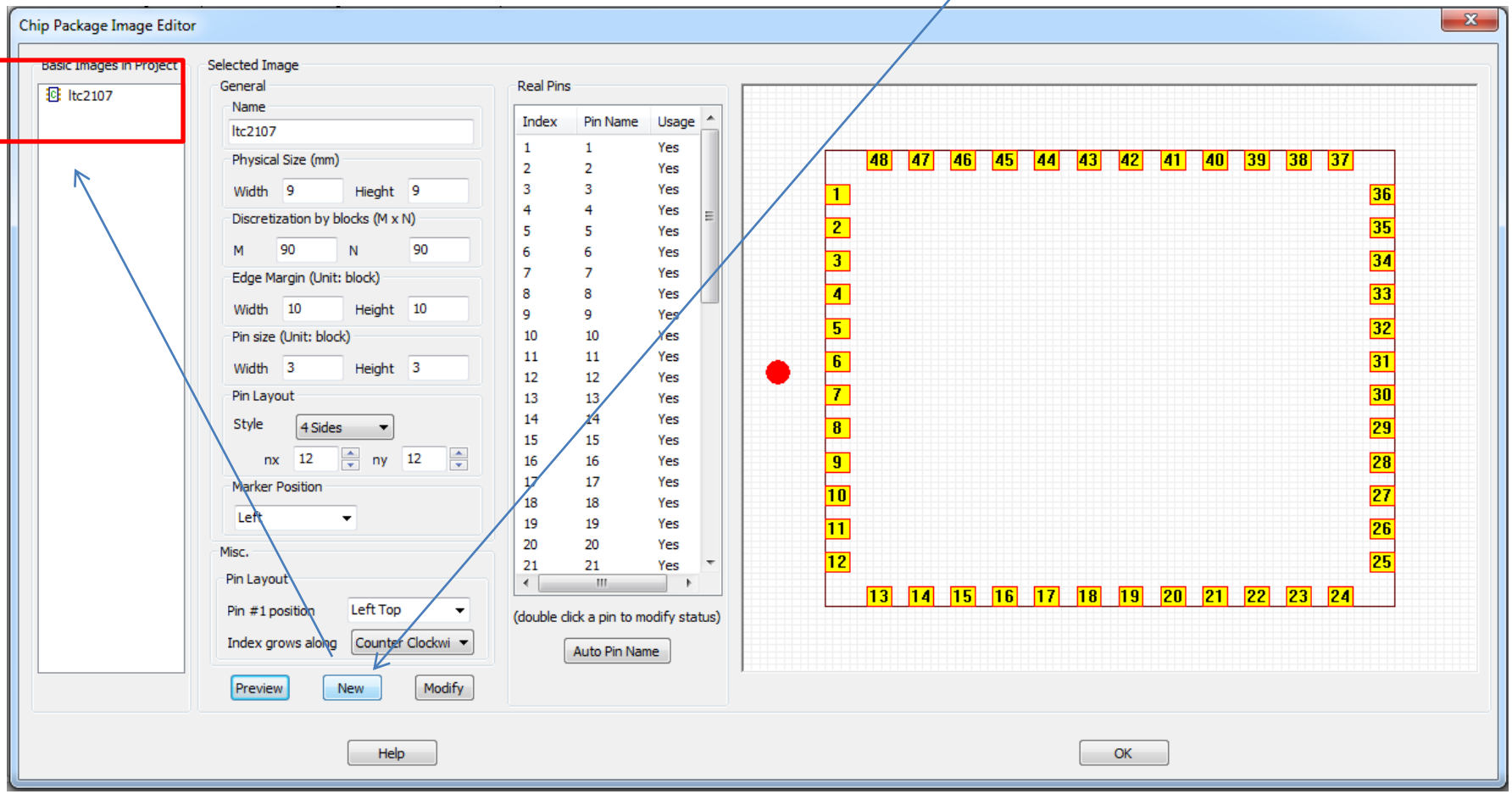
LTC2107 pin configuration figure

In the “Chip Package Image Editor”, input the parameters as following,



Make sure that all input and the figure are correct, press “**New**” button to add this image in the project

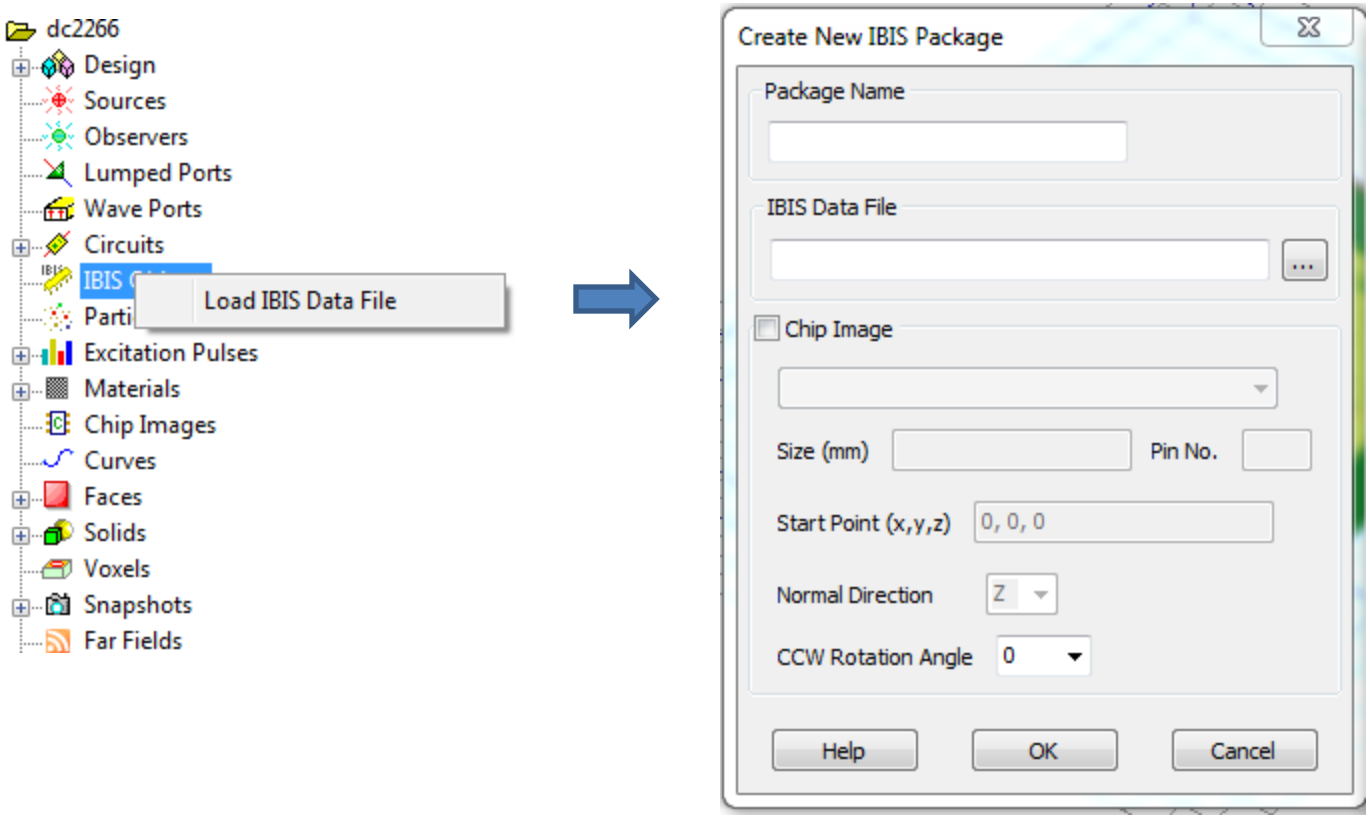
Note: this is the base image for the chip LTC2107. In a project, it can have multiple instances of LTC2107 at different locations. We will show how to use this image in following steps.



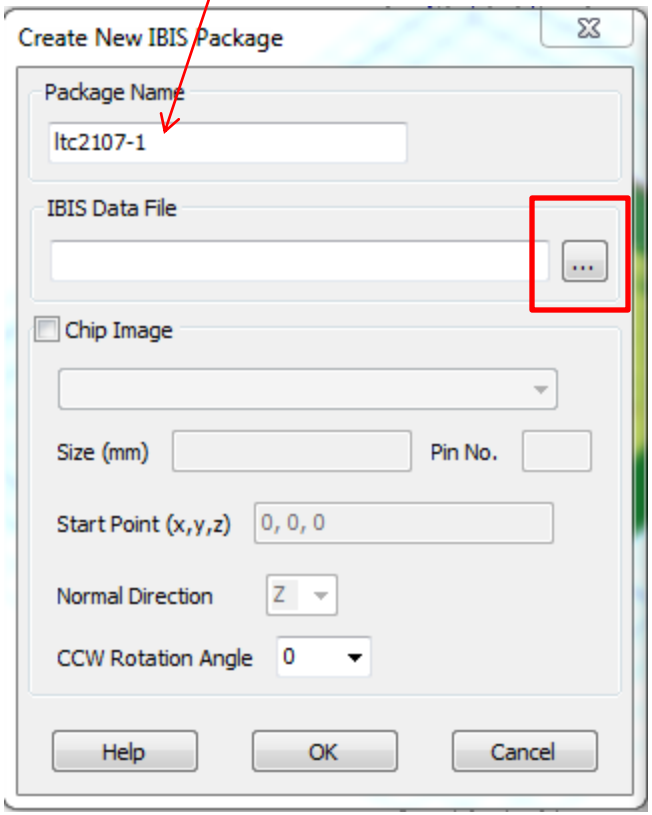
Then “OK” to exit the “Chip Package Image Editor”

Optional 11, Load IBIS data file to make the functionality & the parameters for the pins of LTC2107 readable

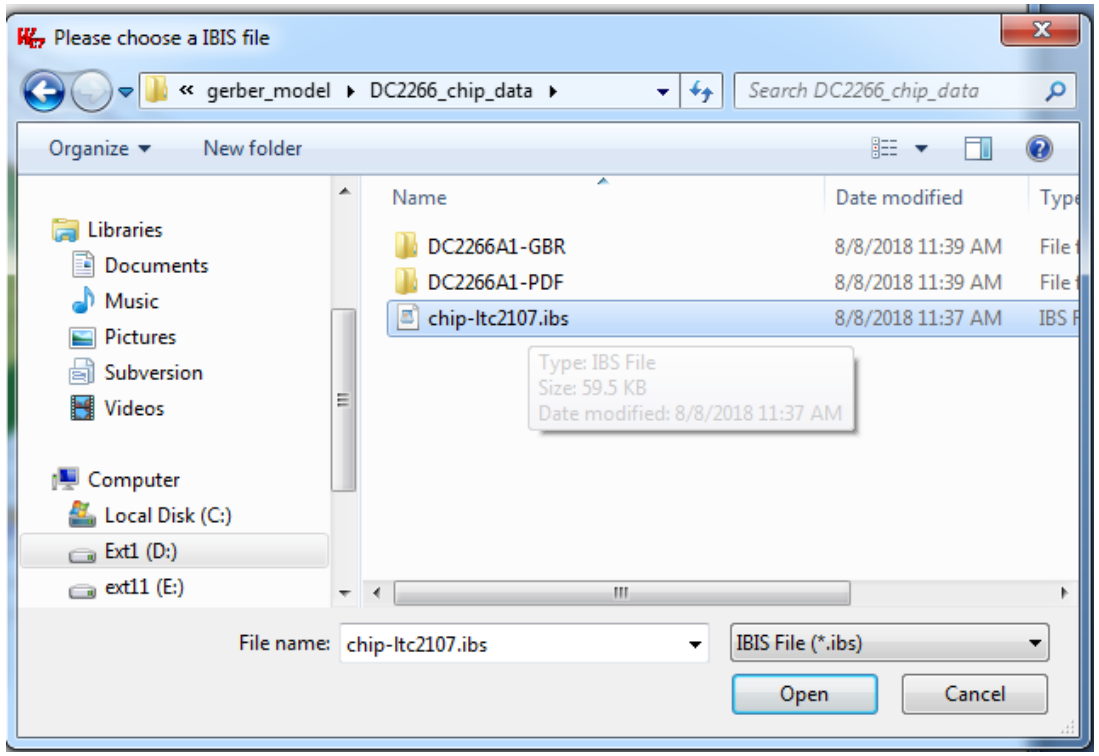
Note: this step is not an essential step for the simulation, it will not affect the simulation result, but will make the model more understandable.

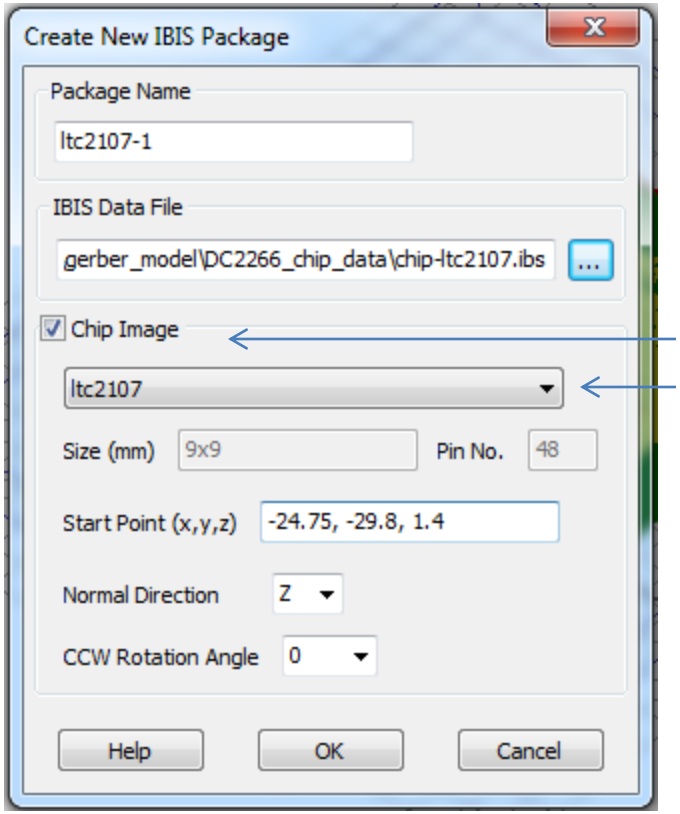


Assign a name to the instance of the chip



Load IBIS data file



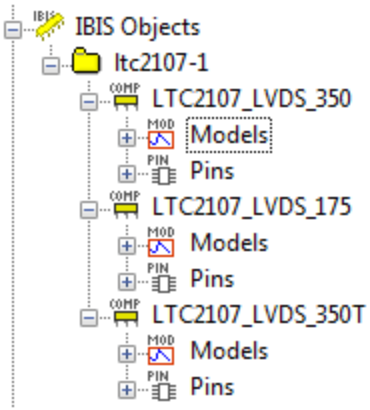


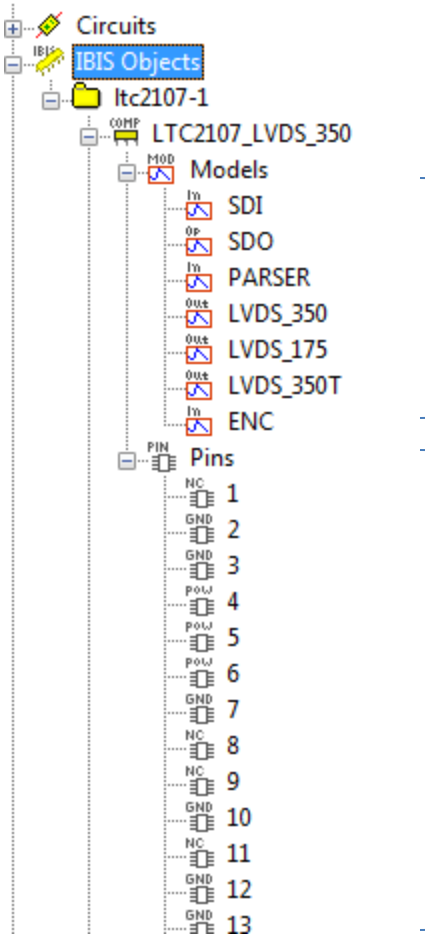
Enable the image of this chip

setup the image for this chip

Image position, etc

After “OK”, the IBIS information of this chip will be added to the project, user can check the information

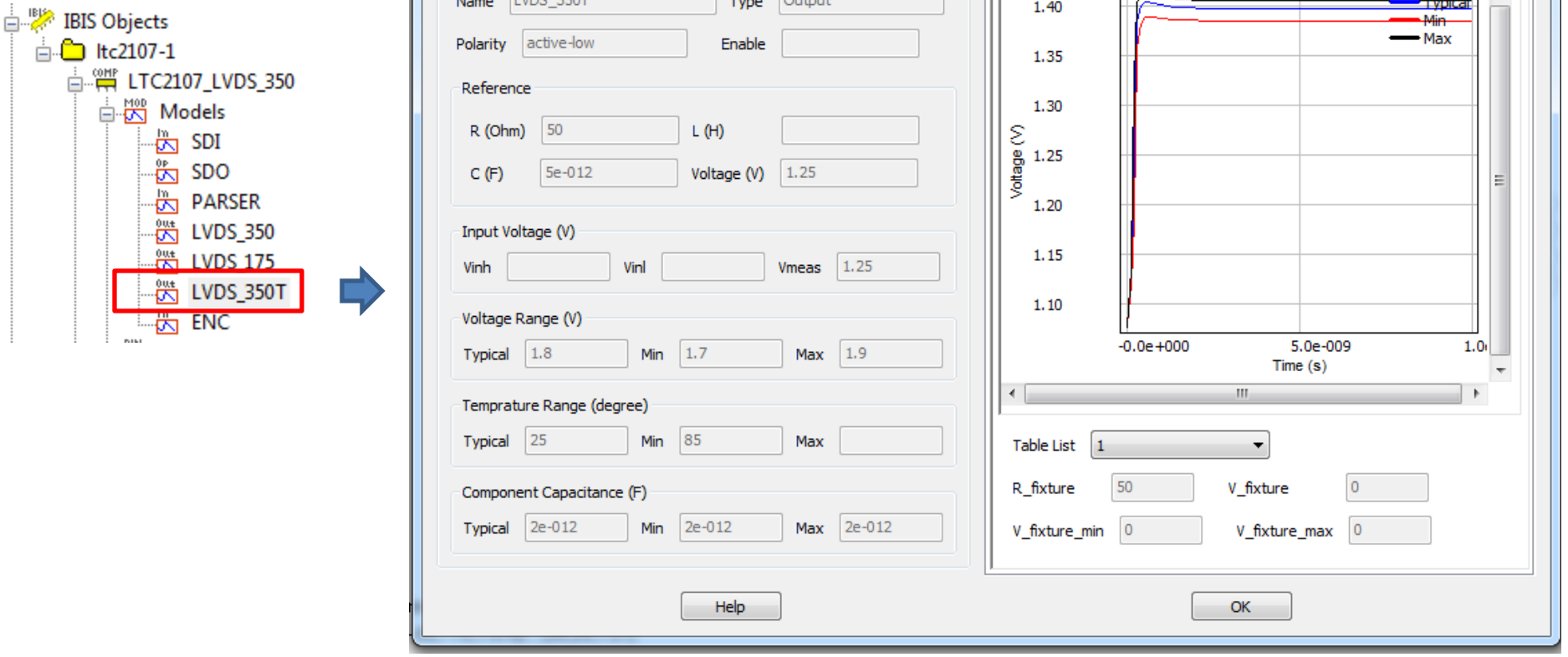




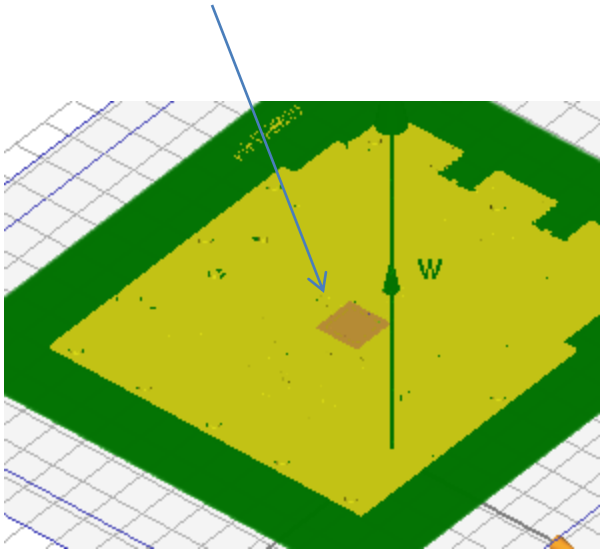
Model types

List of pins, the icon of the pin shows the pin type

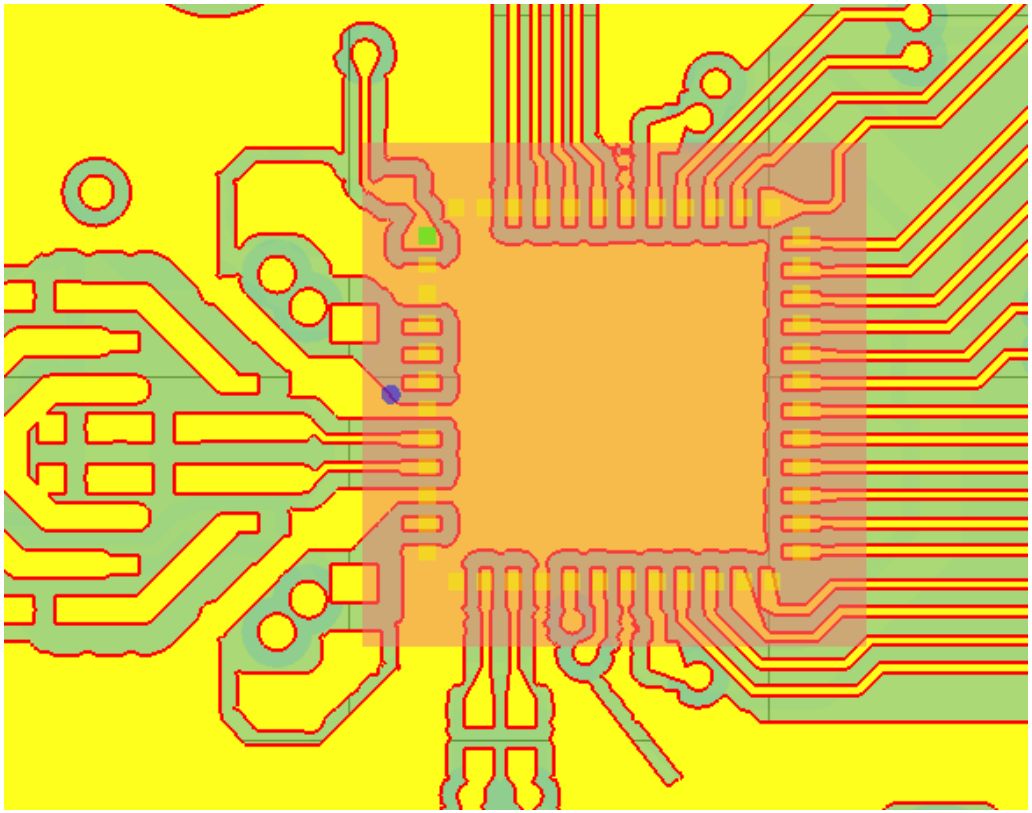
For example, all information of model “LVDS_350T” will be shown by double-click the project tree node “LVDS_350T”



The chip
image in 3D

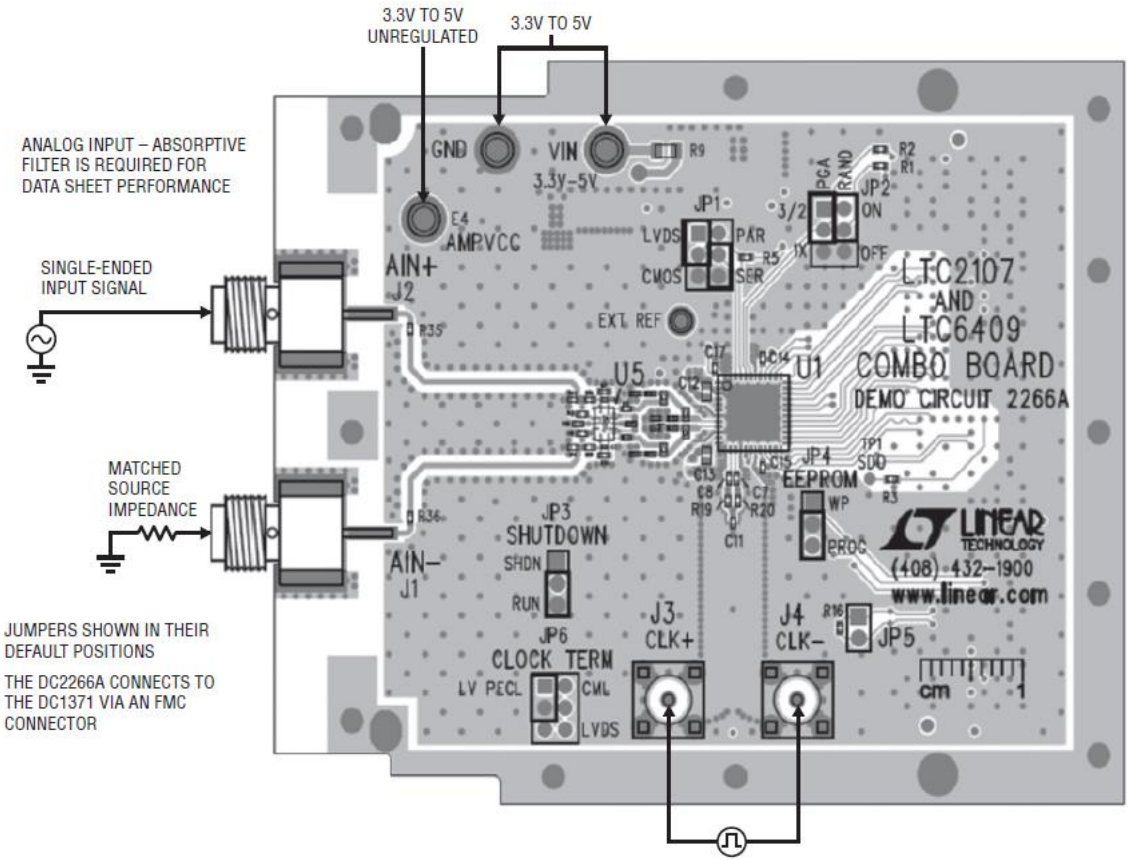


Zoom in the 3D canvas, we can see the image is mapping the pad on PCB correctly. And some pins share the same pad.



12, Add lumped elements in board to make the circuit functional as the design.

Based on the figure in the manual of DC2266A, we can find half of the lumped elements are in the top layer. But more details & the lumped elements in the bottom side need to check the PCB project in the DC2266A design package.



The parameter of lumped elements are listed in the manual of DC2266A.

Part of the Element Table

DEMO MANUAL DC2266A

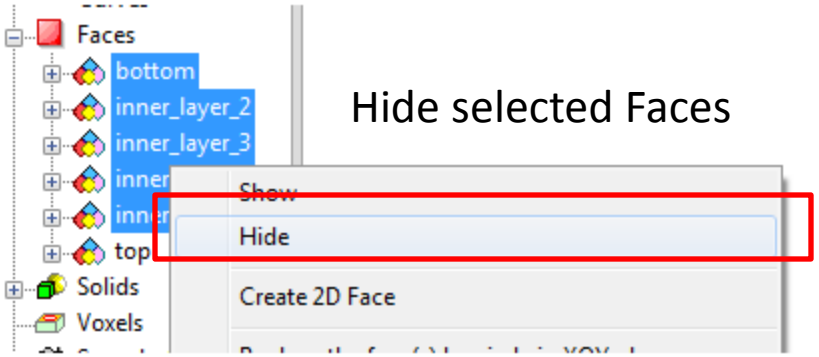
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	2	C1, C24	CAP.,1.5pF, C0G, 50V ±0.25pF, 0201	MURATA, GRM0335C1H1R5CA01D
2	1	C2	CAP., 10µF, X7R, 16V, 10%, 0805	SAMSUNG, CL21B106KOQNNNE
3	2	C3, C12	CAP., 1µF, X5R, 25V, 10%, 0603	TDK, C1608X5R1E105K080AC
4	4	C4, C9, C16, C20	CAP., 10µF, X5R, 16V, 20%, 1206	TDK, C3216X5R1C106M
5	2	C5, C6	CAP., 100µF, X5R, 16V, 20%, 1210	TAIYO YUDEN, EMK325ABJ107MM-T
6	2	C7, C8	CAP., 2200pF, C0G, 25V, 5%, 0402	KEMET, C0402C222J3GACTU
7	3	C10, C26, C27	CAP., 0.1µF, X7R, 50V, 10%, 0402	TDK, C1005X7R1H104K
8	4	C11, C14, C15, C23	CAP., 0.1µF, X5R, 16V, 10%, 0402	AVX, 0402YD104KAT2A
9	1	C13	CAP., 2.2µF, X5R, 16V, 20%, 0603	AVX, 0603YD225MAT2A
10	1	C17	CAP., 2.2µF, X5R, 16V, 20%, 0402	TDK, C1005X5R1C225M050BC
11	0	C18	CAP., OPTION, 0402	OPTION
12	1	C19	CAP., 47µF, X5R, 16V, 20%, 1206	TDK, C3216X5R1C476M160AB
13	4	C21, C22, C25, C28	CAP., 4.7pF, NP0, 50V, ±0.25pF, 0402	TDK, C1005C0G1H4R7C
14	1	E1	TEST POINT, TURRET, 0.064" MTG. HOLE	MILL-MAX, 2308-2-00-80-00-00-07-0
15	3	E2, E3, E4	TEST POINT, TURRET, 0.094" MTG.HOLE	MILL-MAX, 2501-2-00-80-00-00-07-0
16	3	JP1, JP2, JP6	CONN., HEADER, 2 × 3, 2mm, THRU-HOLE, VERTICAL	SAMTEC, TMM-103-02-L-D
17	2	JP3, JP4	CONN., HEADER, 1 × 3, 2mm, THRU-HOLE, VERTICAL	SAMTEC, TMM-103-02-L-S

User can define these lumped R, L, C in the ***top*** & ***bottom*** PCB layers.

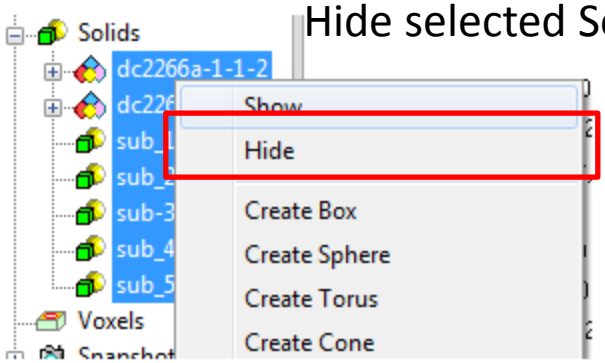
Note:
When defining the lumped elements, we skip all Jumpers. This is because the jumper can be set as open or short, it depends on the configuration. Here, we assume all jumpers are set as open.

In defining the Lumped element, for example, the elements in the ***top*** PCB layer, we suggest to "***HIDE***" all un-related PCB layers, substrates and via. It is because we use 0-thickness faces to represent the PCB layers, which will have the same Z position of some faces of substrate & via, it will mess up the selected objects in hitting the screen if all 3 types of objects has the same Z positions.

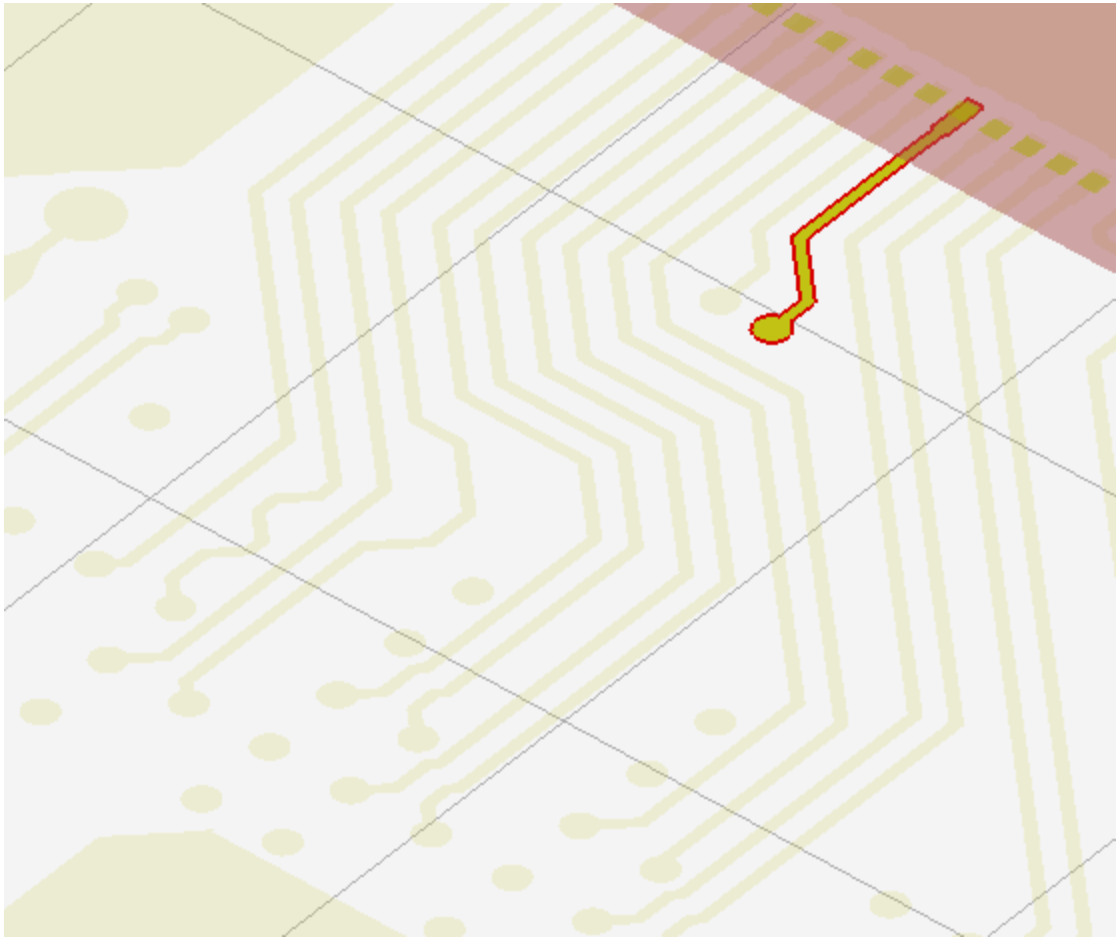


Hide selected Faces

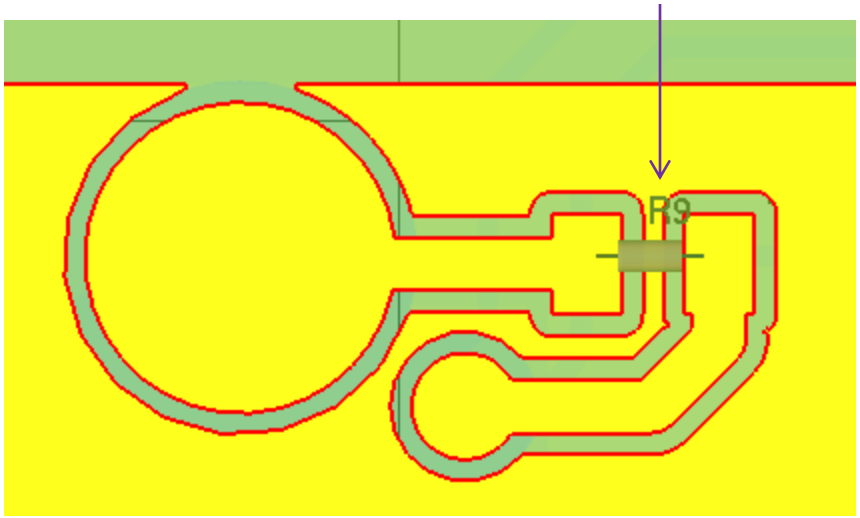
Hide selected Solids



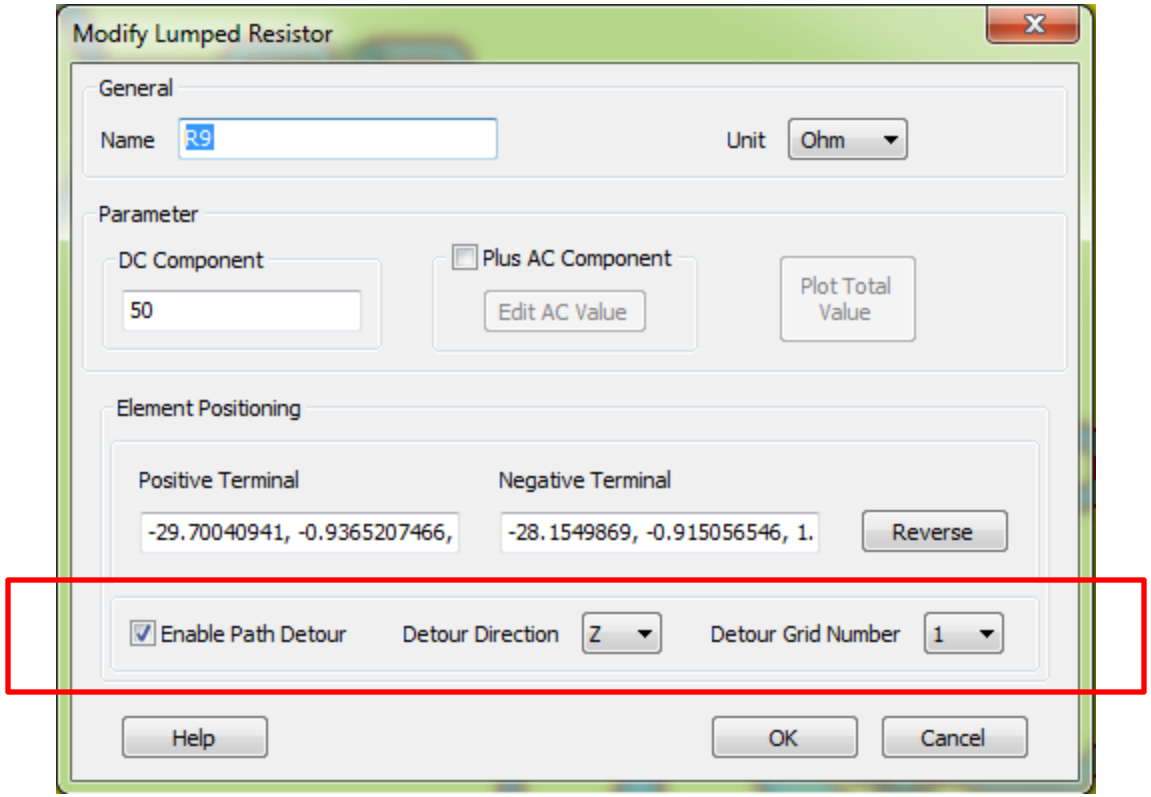
Here, only the objects in the “Top” PCB layer are shown.



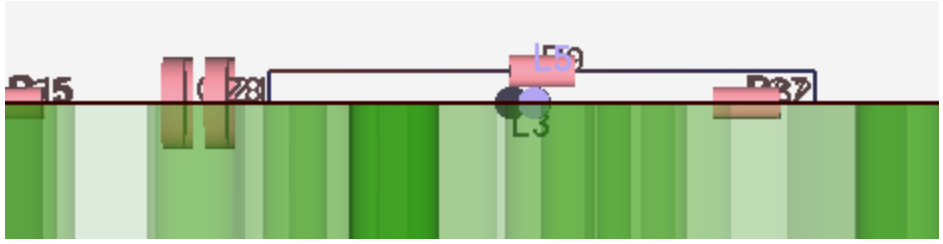
One special lumped resistor need to be mentioned is ***R9***, there is a trace between the two terminals of this resistor.



So, this lumped resistor need to enable "path detour" function, which will rise the path of this lumped resistor to avoid touching the trace in the middle.

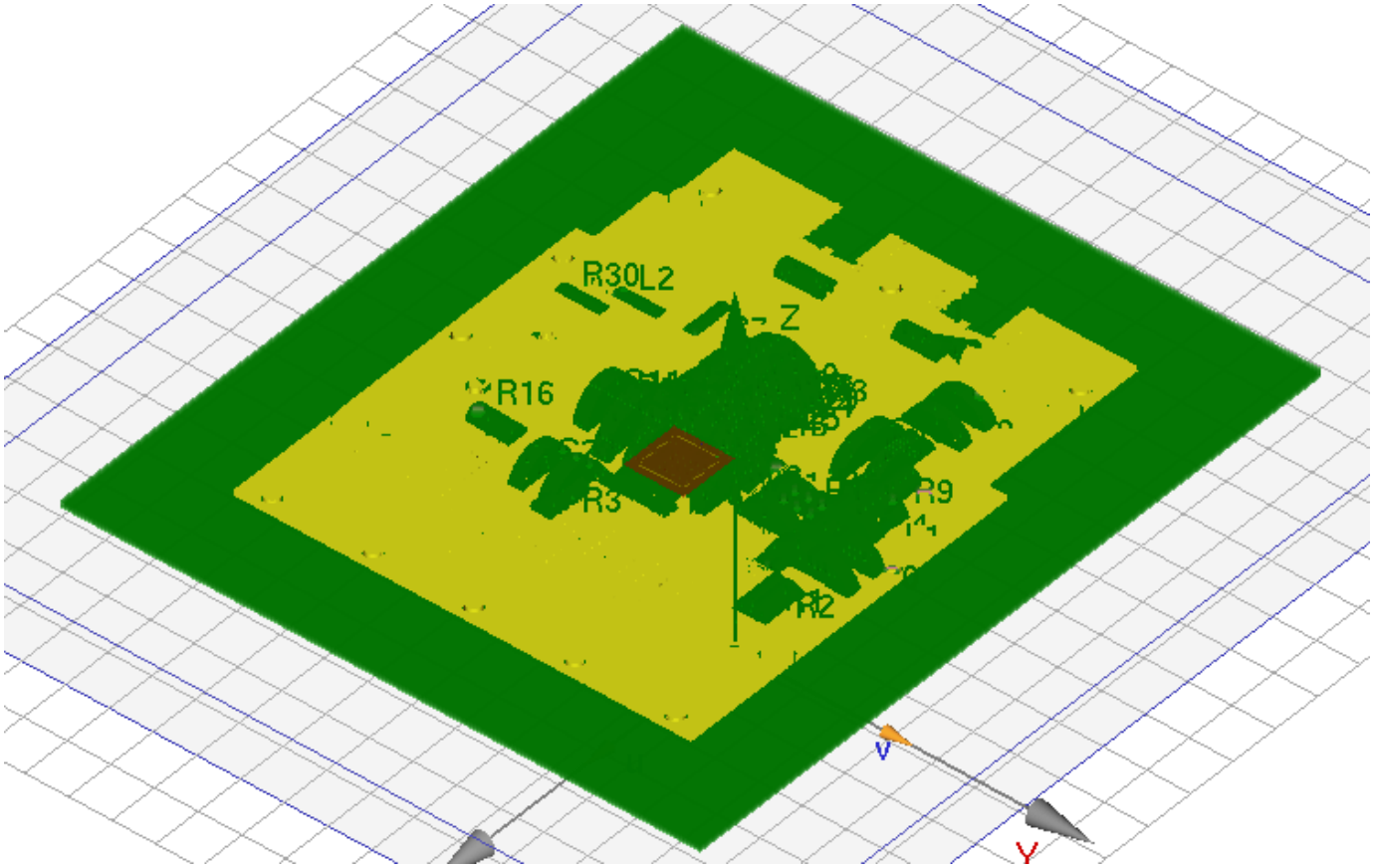


In 3D view, the path of R9 will be as the right figure.

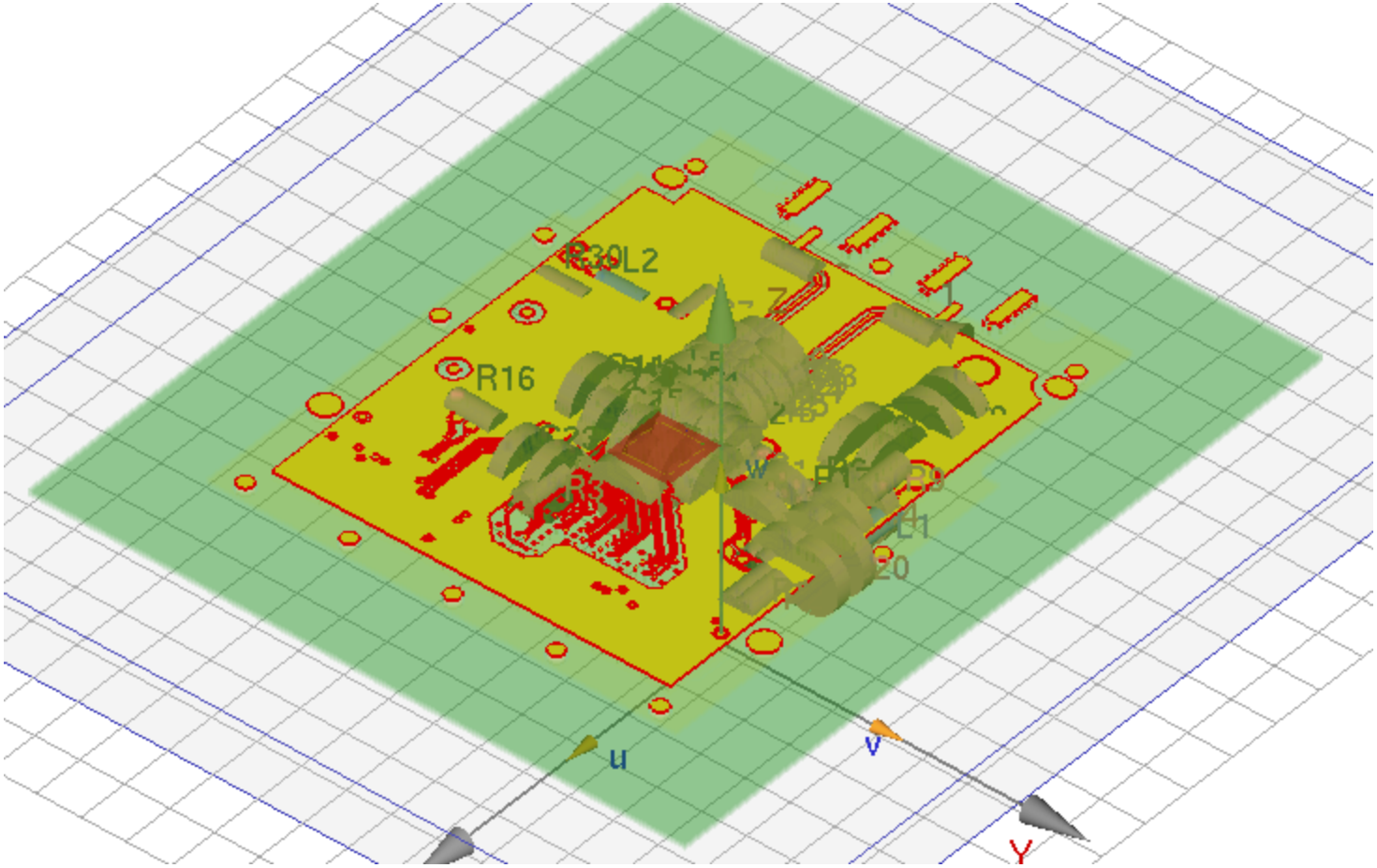


Path detour in +Z direction as user input

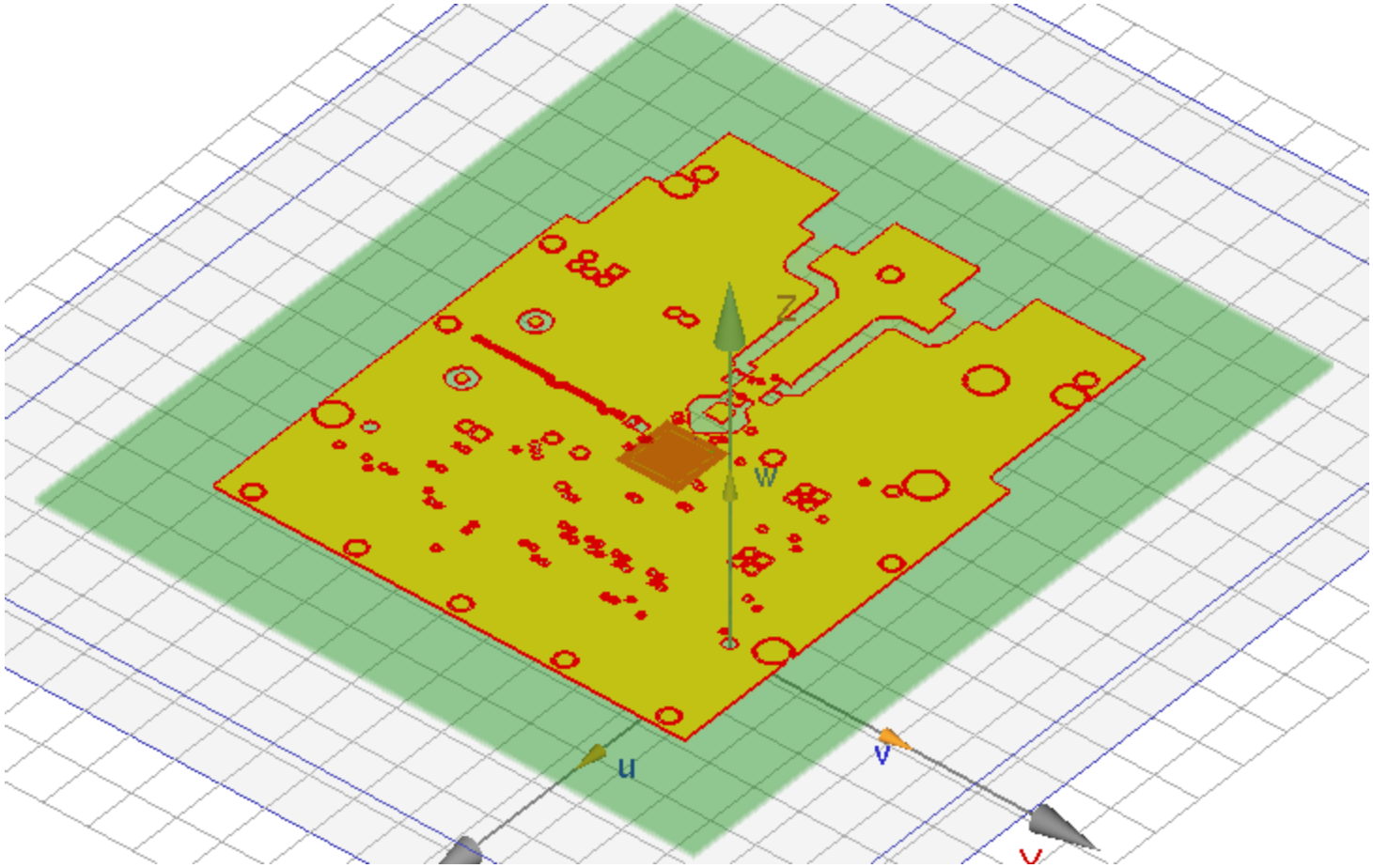
After all lumped elements are set, the simulation set up of the project is almost finished, the project in 3D view is as following,



The top layer PCB is as

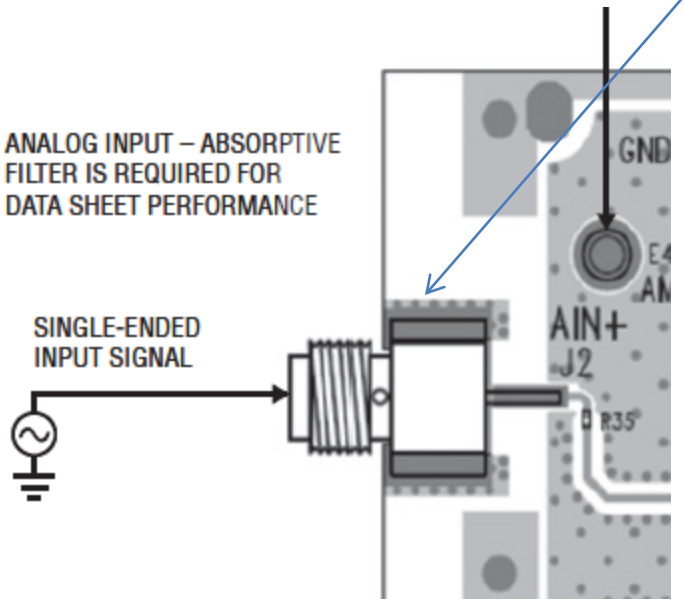


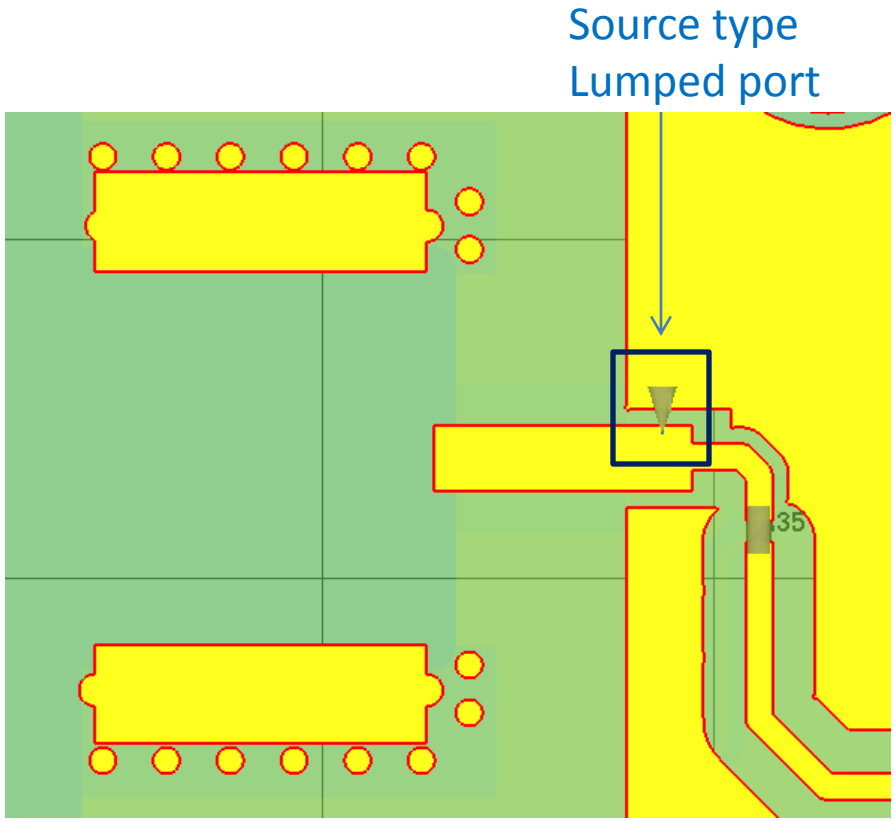
The 2nd layer PCB is as



13. Add input signal

From the manual of DC2266A, the input signal will be as the left figure.
Because we don't build the model for the connector, we define a lumped port to connect the signal trace & ground to input the signal as the right figure.



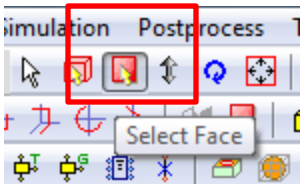


14. Define face snapshots to record the current in each PCB layer

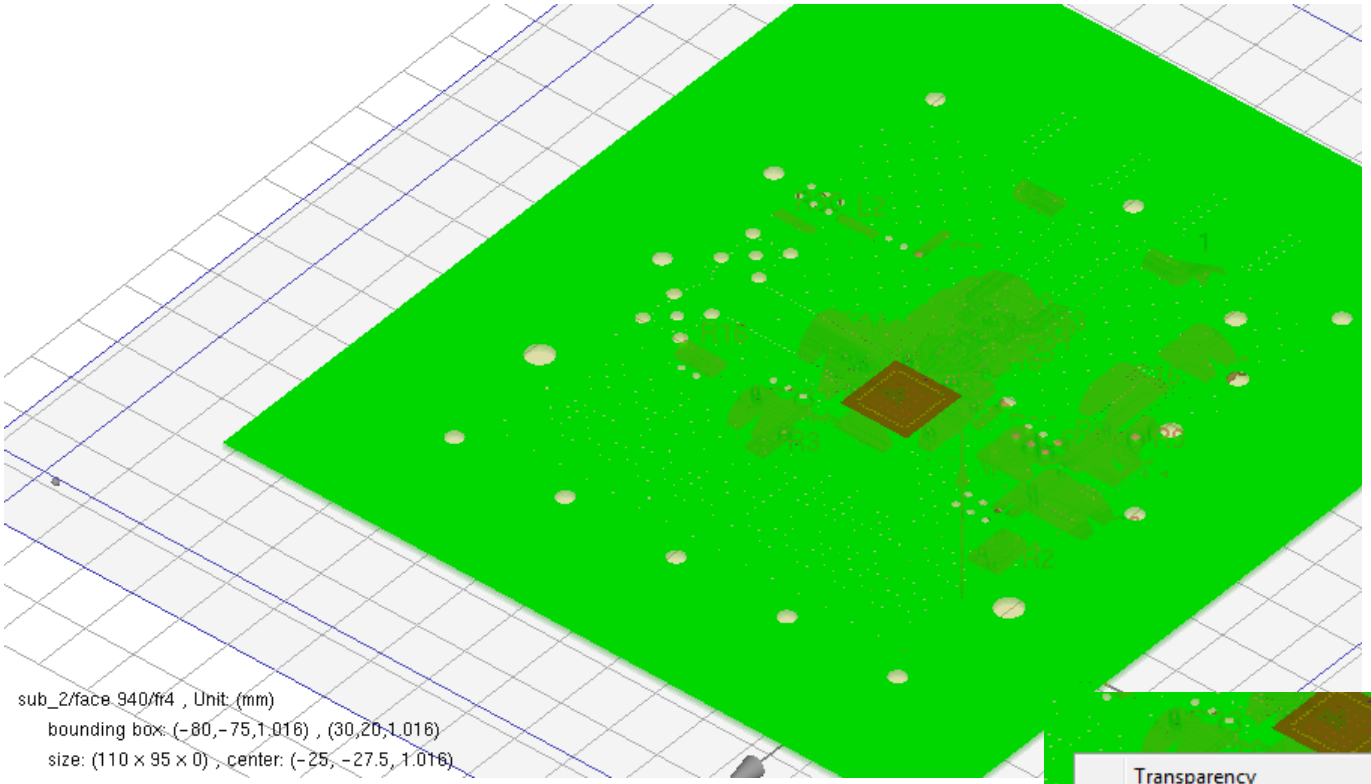
For example, user want to define a face snapshots to record the current in PCB layer 2.

The PCB layer 2 is at the bottom Z face of **sub_1**, it also is at the top Z face of **sub_2**.

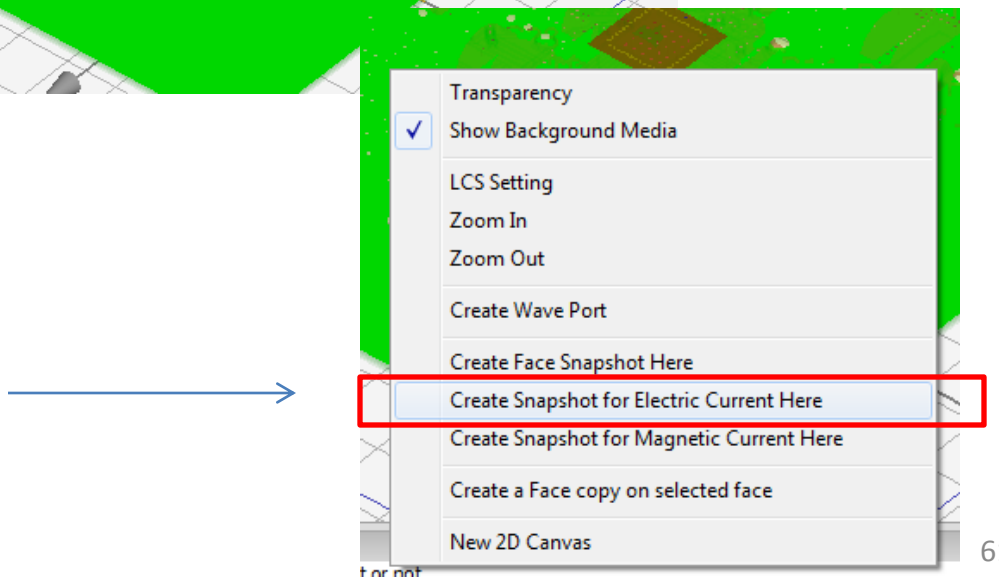
So, for simplicity, user “Hide” **sub_1**, then enter “Select Face” mode,



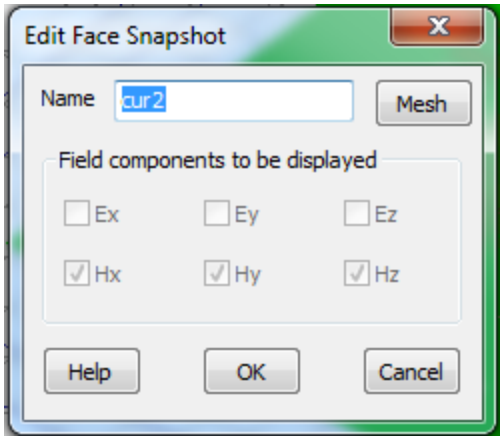
Hit the top Z face of sub_2 to select it.



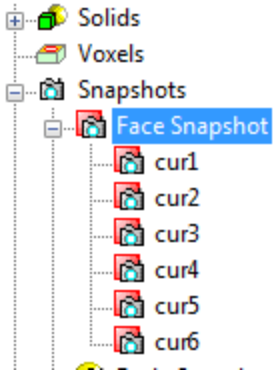
Then right click the mouse button to popup the menu, and define a face snapshot to record the current on the selected face



E current snapshot for PCB layer 2



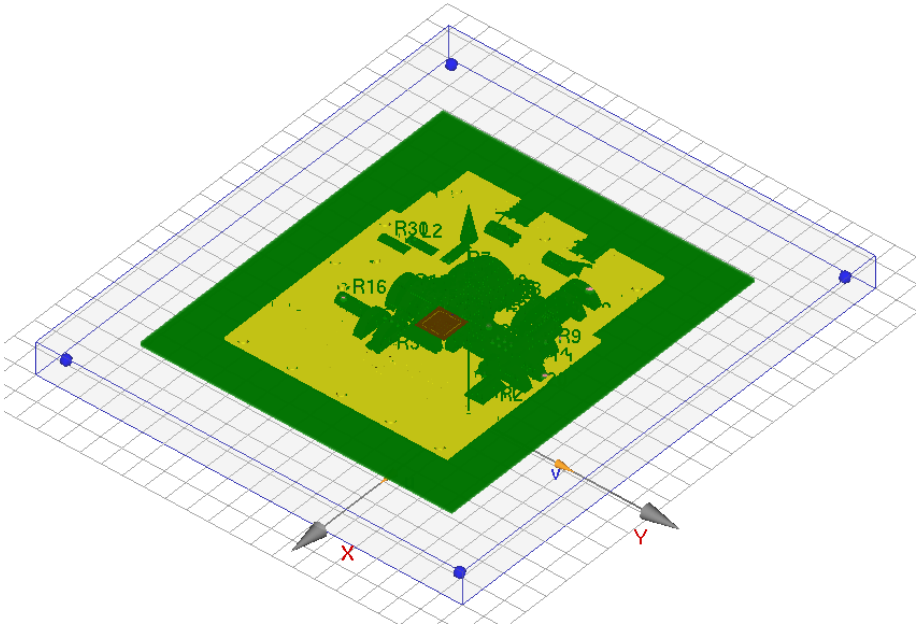
In this case, we define 6 face snapshots to record the current in 6 PCB layers.



Optional 15. Define 4 receivers at the computational domain corners to monitor the field.

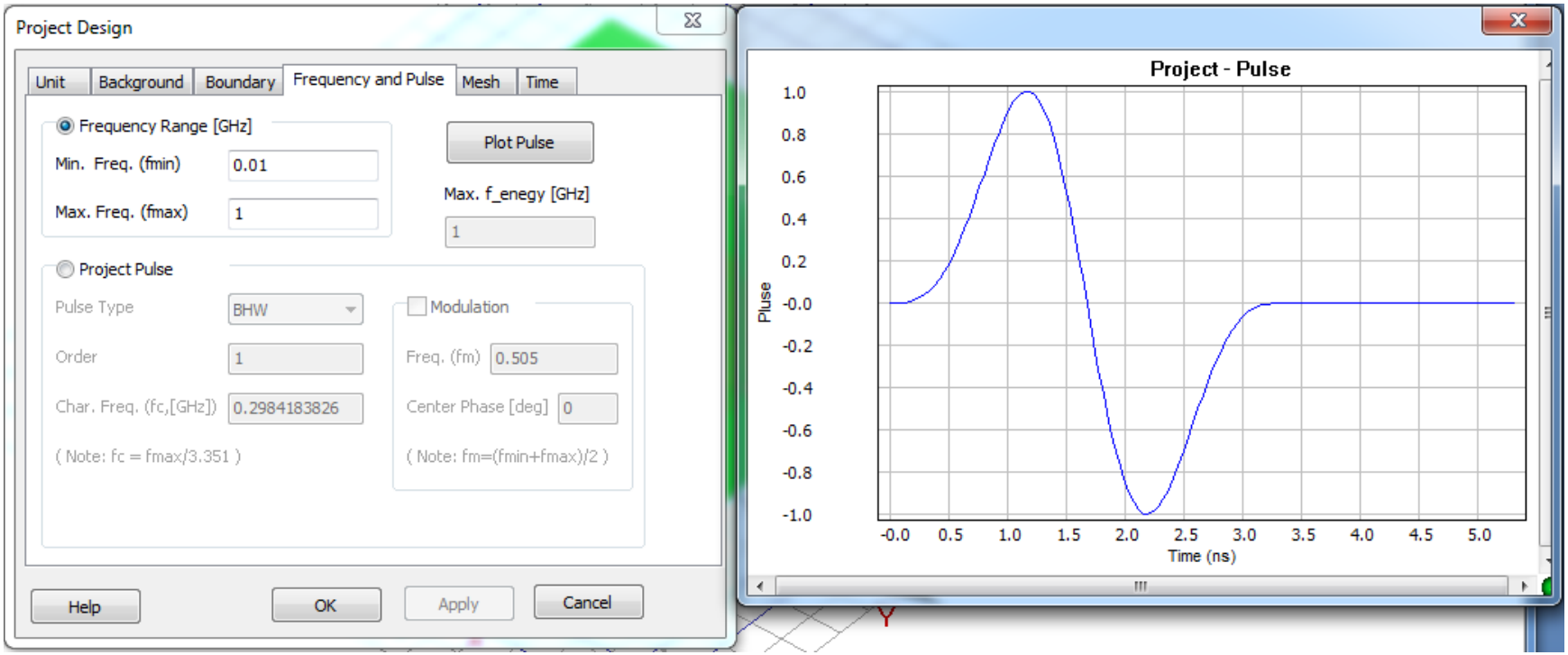
This is because we don't know how the signal propagates in the board. So, we can't estimate how long time the simulation will run to get the final convergence status. With these receivers, we can check the field magnitude dynamically in the simulation and determine whether we can stop the simulation before it reach the final convergence status.

This is an optional step, user still can use automatic simulation time window without defining receivers to simulate this project.



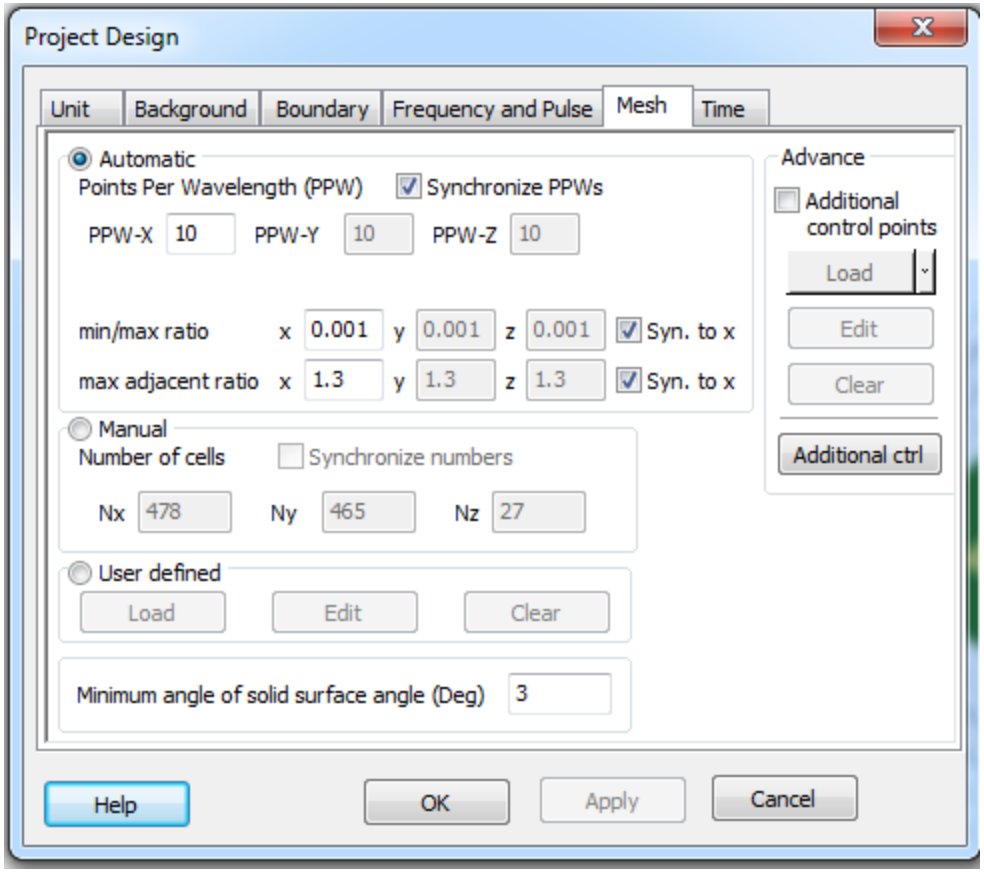
16. Check excitation signal before the simulation

Here, the excitation pulse will be a BHW wideband signal with f_{max}=1 GHz.

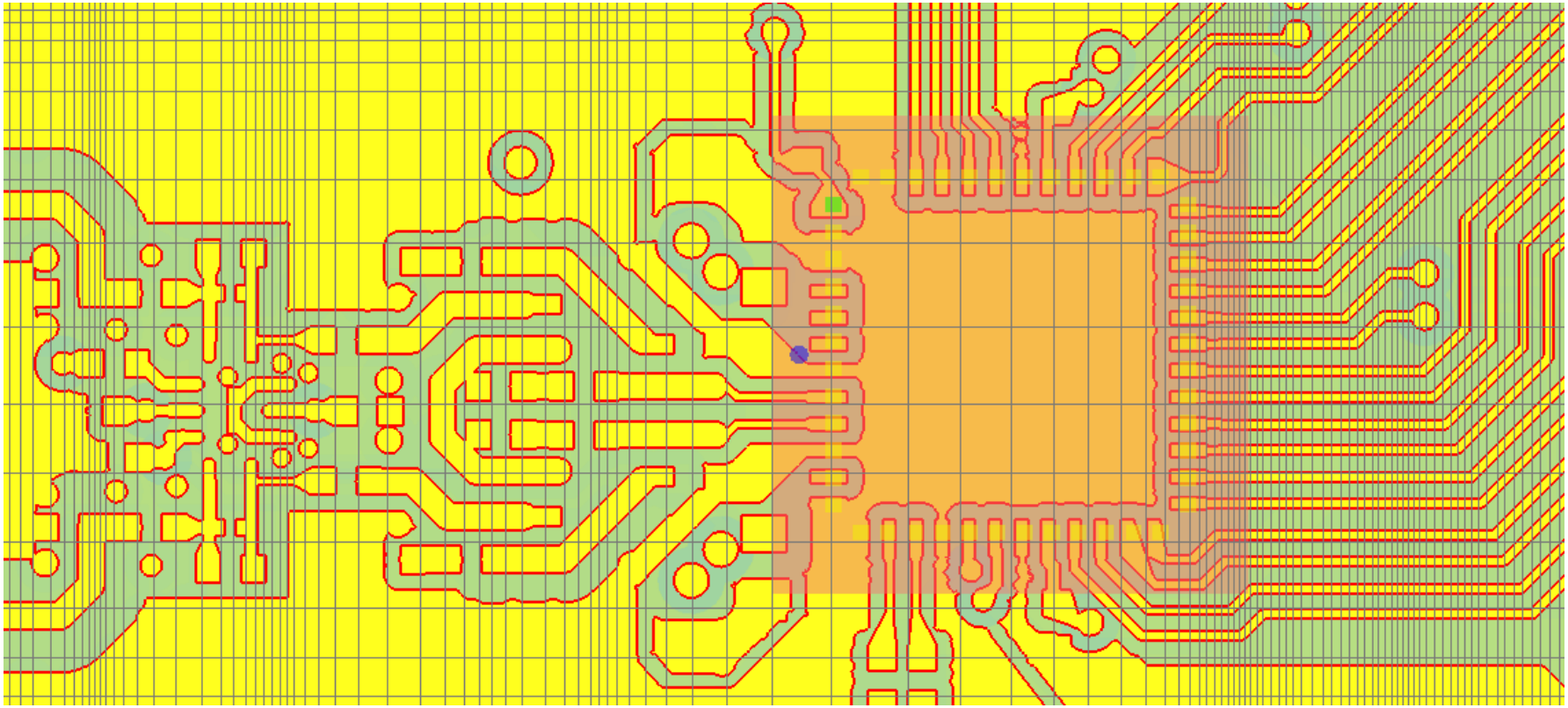


17. Check the mesh quality

The default setting is PPW=10

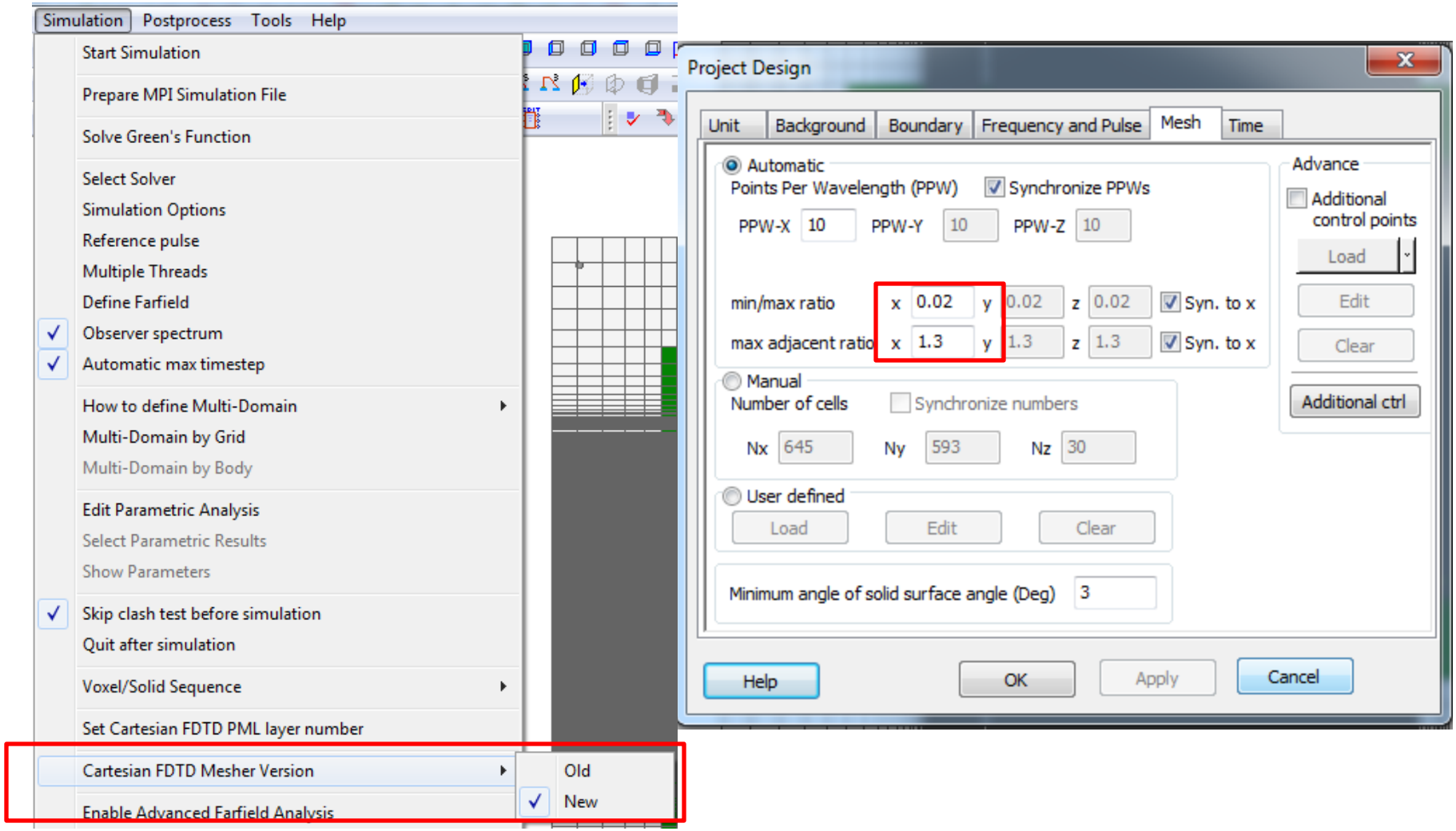


It can be seen that many traces
are not captured by grid correctly.

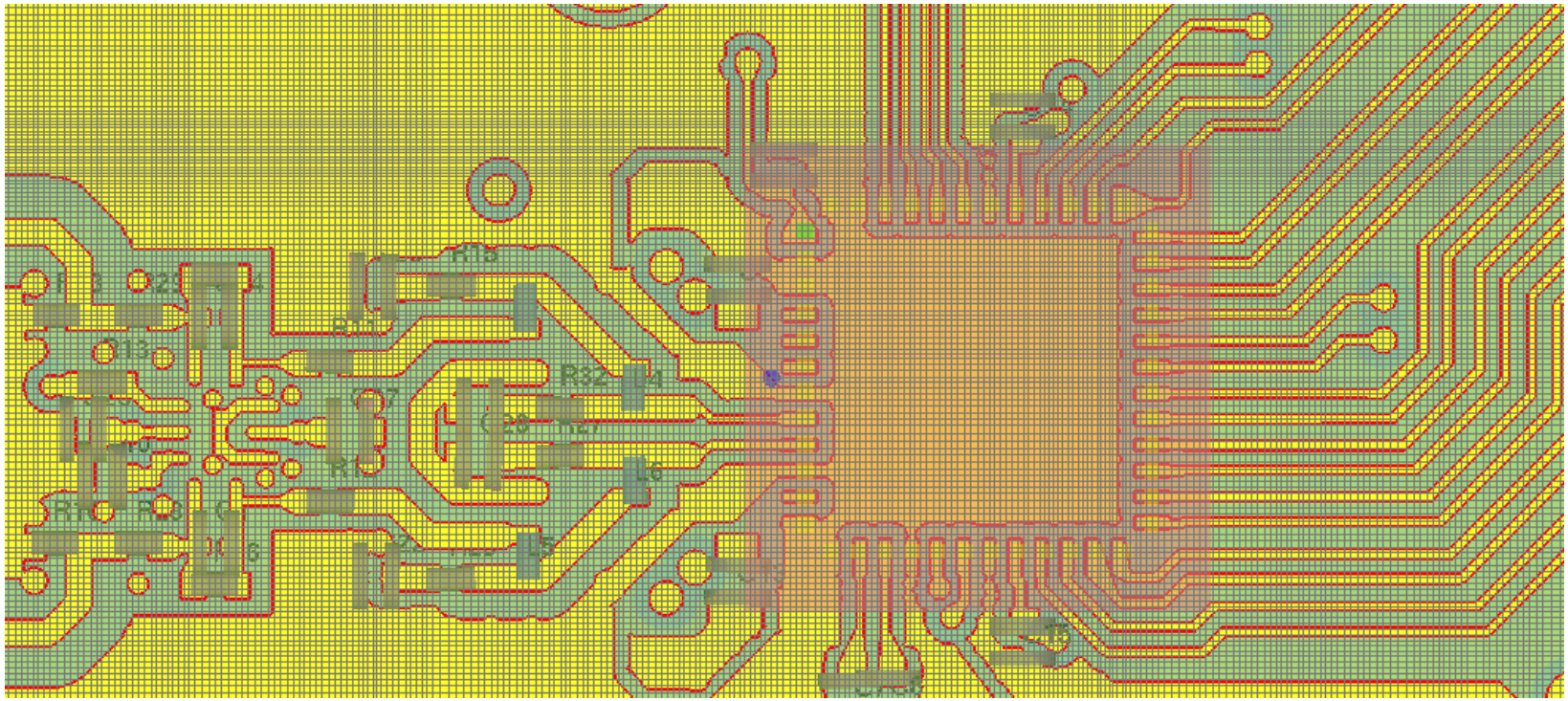


We switch to the “New” mesher

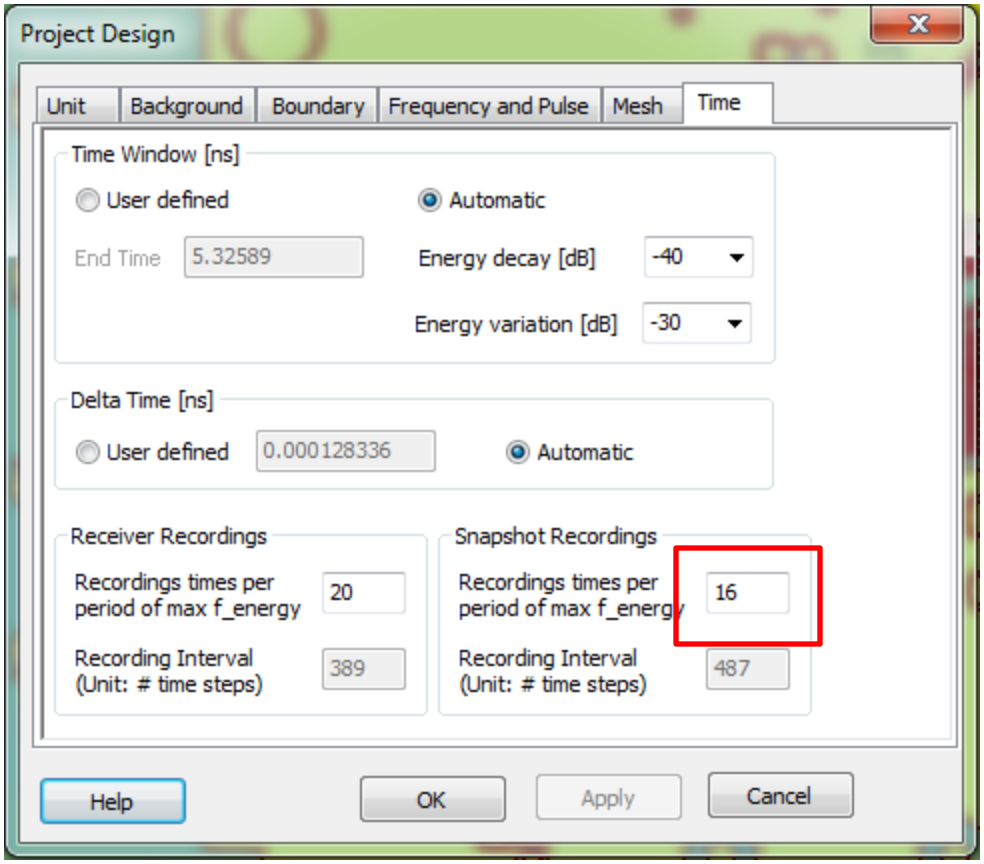
Set up the mesh control as following



It can be seen that traces can be captured by grid correctly.



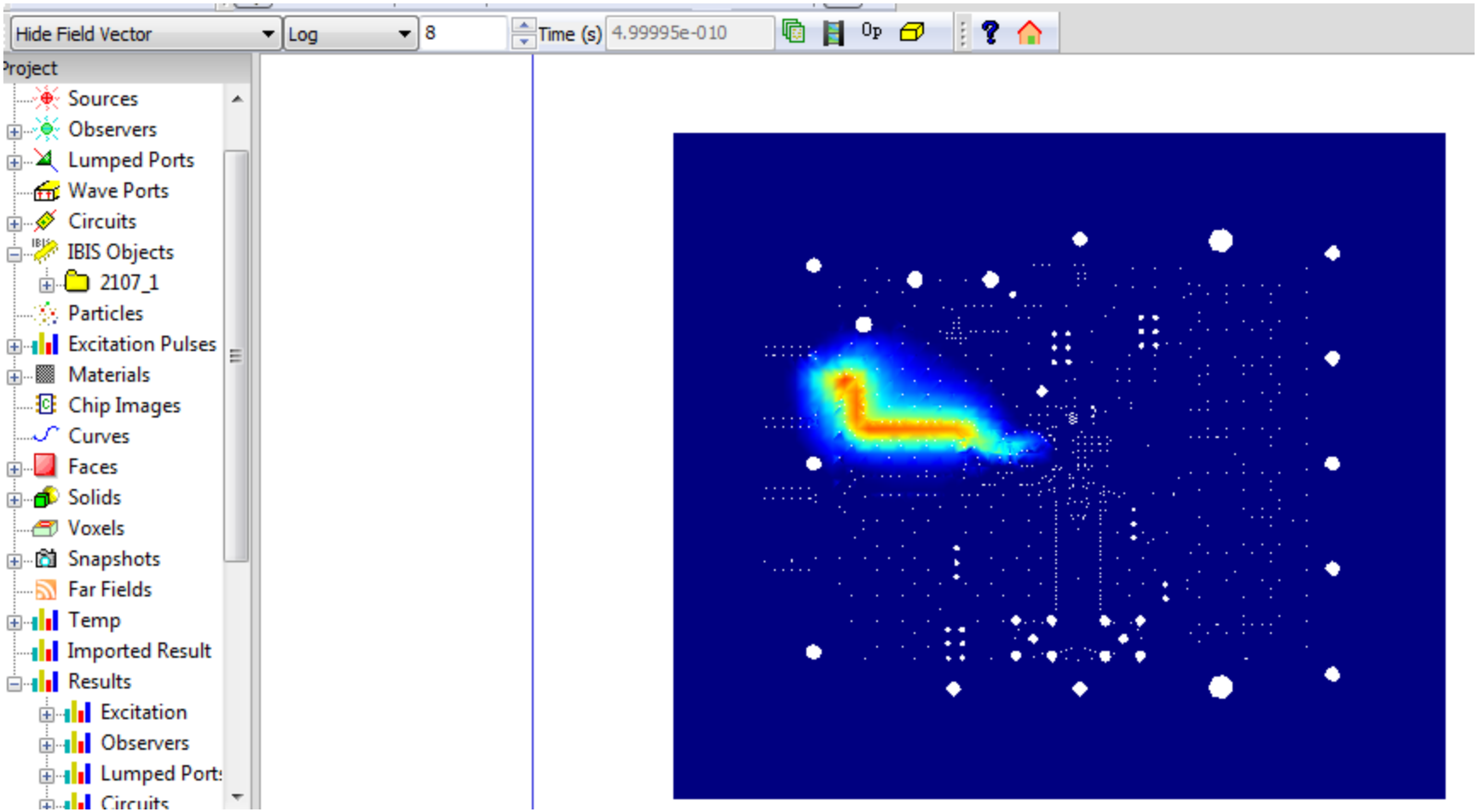
18. Check the time setting



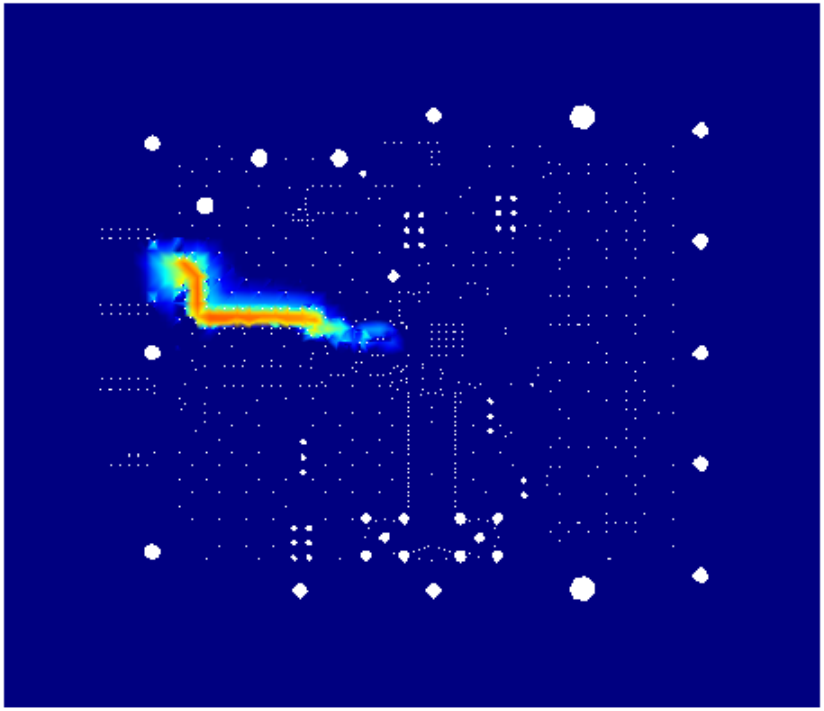
Set snapshot recording interval as 16 recorders per period

19. Start Simulation & check result

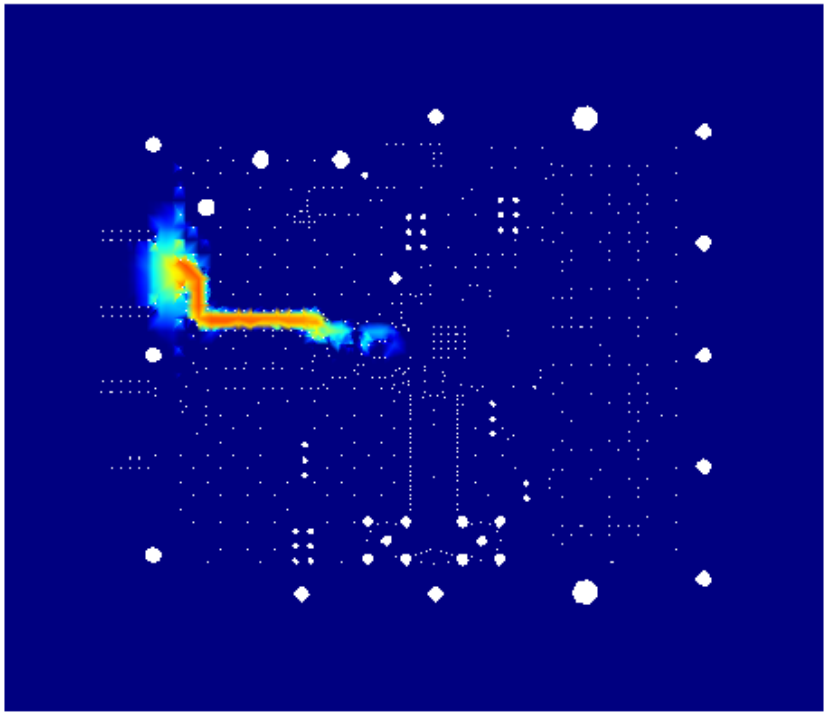
E Current in the snapshot for the top layer



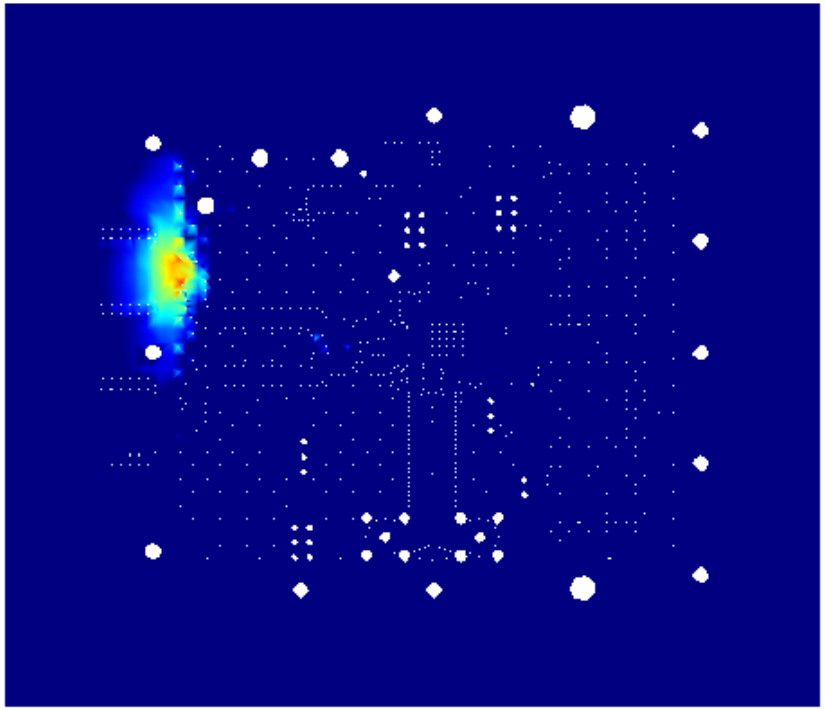
E Current in the snapshot for 2nd layer



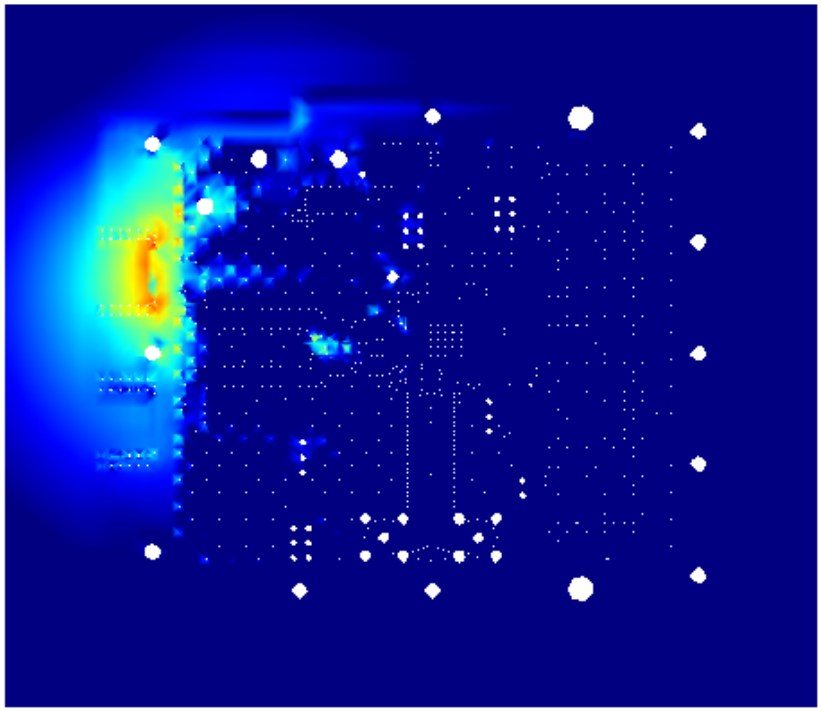
3rd layer



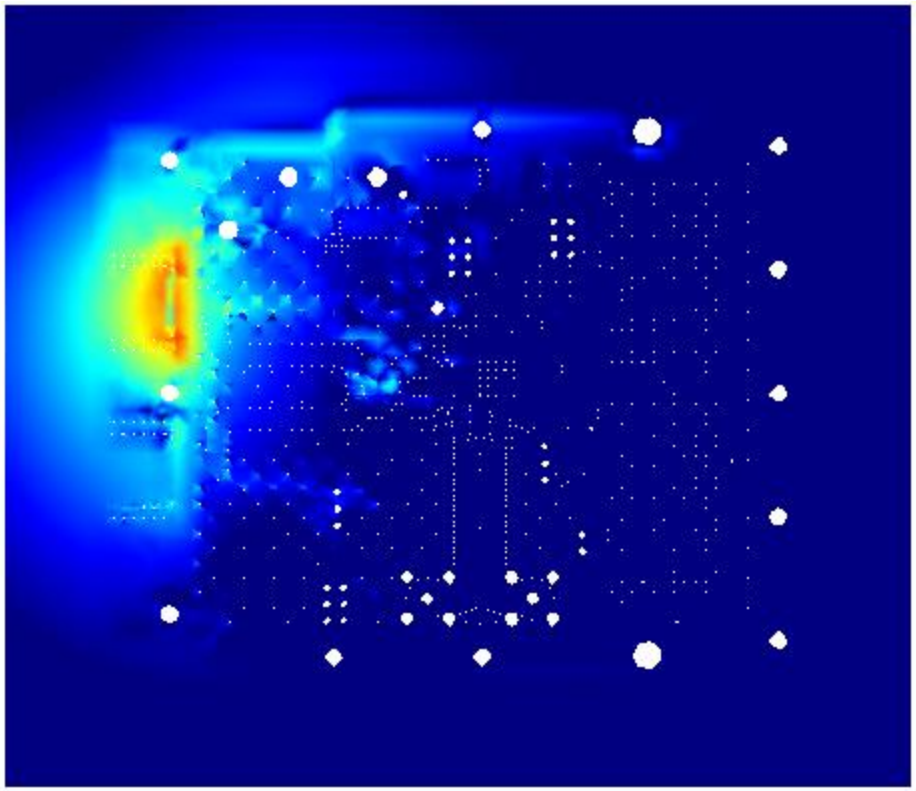
4th layer



5th layer



Bottom layer



As can be seen, the input signal is totally being isolated from layer 4.

User also can check the S parameter of the lumped port, or add farfield monitor to check the radiation of the board. These depend on user requirements, and are not discussed in this demo.